SONY

Diagonal 6.52 mm (Type 1/2.8) CMOS Solid-state Image Sensor with Square Pixel for Color Cameras

Tentative

IMX335LQN-C

STARVIS

Description

The IMX335LQN-C is a diagonal 6.52 mm (Type 1/2.8) CMOS active pixel type solid-state image sensor with a square pixel array and 5.14 M effective pixels. This chip operates with analog 2.9 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color mosaic filters. This chip features an electronic shutter with variable charge-integration time.
(Applications: Surveillance cameras, FA cameras, Industrial cameras)

Features

- ◆CMOS active pixel type dots
- ◆Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆Input frequency: 6 to 27 MHz / 37.125 MHz / 74.25 MHz
- ◆Number of recommended recording pixels: 2592 (H) × 1944 (V) approx. 5.04M pixel
- ◆Readout mode
  All-pixel scan mode
  Horizontal/Vertical 2/2-line binning mode
  Window cropping mode
  Vertical / Horizontal direction-normal / inverted readout mode
- ◆Readout rate
  Maximum frame rate in All-pixel scan mode 2592(H)×1944(V) AD10bit: 60 frame / s
- ◆Wide dynamic range (WDR) function
  Multiple exposure WDR
  Digital overlap WDR
- ◆Variable-speed shutter function (resolution 1H units)
- ◆10-bit / 12-bit A/D converter
- ◆CDS / PGA function
  0 dB to TBDdB (step pitch 0.3 dB)
  Supports I/O
  CSI-2 serial data output (2 Lane / 4 Lane, RAW10 / RAW12 output)
- ◆Recommended exit pupil distance: –30 mm to –∞

Exmor R

Device Structure

- CMOS image sensor
- Image size
  Type 1/2.8
- Total number of pixels
  2704 (H) × 2104 (V) approx. 5.69 M pixels
- Number of effective pixels
  2616 (H) × 1964 (V) approx. 5.14 M pixels
- Number of active pixels
  2608 (H) × 1960 (V) approx. 5.11 M pixels
- Number of recommended recording pixels
  2592 (H) × 1944 (V) approx. 5.04 M pixels
- Unit cell size
  2.0 µm (H) × 2.0 µm (V)
- Optical black
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 13 pixels, rear 0 pixels
- Dummy
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 0 pixels, rear 0 pixels
- Substrate material
  Silicon

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (analog 1 : 2.9 V)	AV_{DD1}	-0.3	3.3	V	
Supply voltage (analog 2 : 2.9 V)	AV_{DD2}	-0.3	3.3	V	
Supply voltage (interface 1.8 V)	OV_{DD}	-0.3	3.3	V	
Supply voltage (digital1 : 1.2 V)	DV_{DD1}	-0.3	2.0	V	
Supply voltage (digital 2 : 1.2 V)	DV_{DD2}	-0.3	2.0	V	
Input voltage	VI	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V

Application Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog 1 : 2.9 V)	AV_{DD1}	2.80	2.90	3.00	V
Supply voltage (analog 2 : 2.9 V)	AV_{DD2}	2.80	2.90	3.00	V
Supply voltage (interface 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (digital1 : 1.2 V)	DV_{DD1}	1.10	1.20	1.30	V
Supply voltage (digital 2 : 1.2 V)	DV_{DD2}	1.10	1.20	1.30	V
Performance guarantee temperature	Tspec	-10	—	60	˚C
Operating guarantee temperature	Topr	-30	—	TBD	˚C
Storage guarantee temperature	Tstg	-40	—	85	˚C

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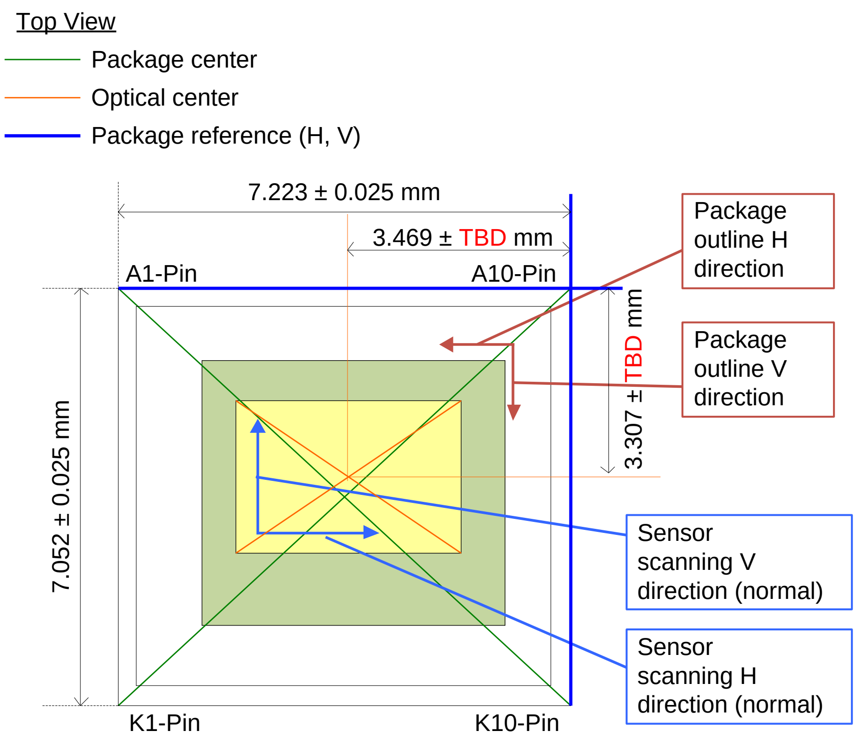
General-0.0.9

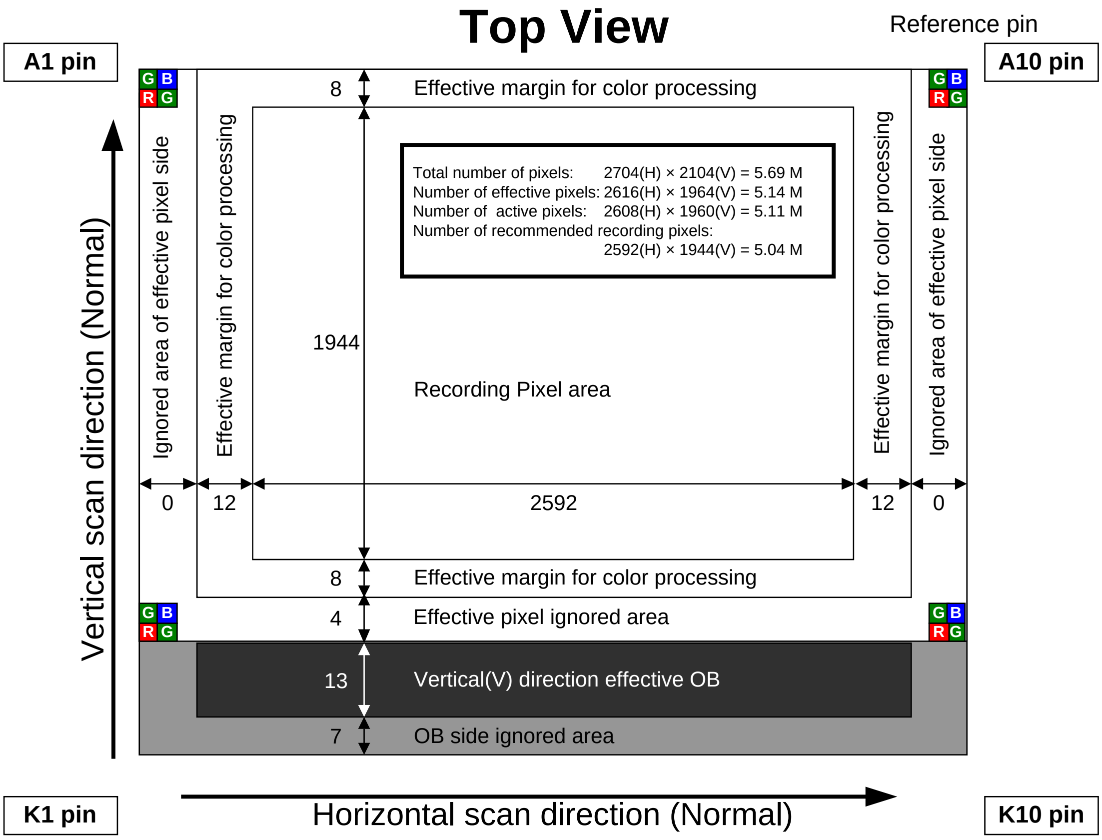
Contents

Optical Center



Optical Center

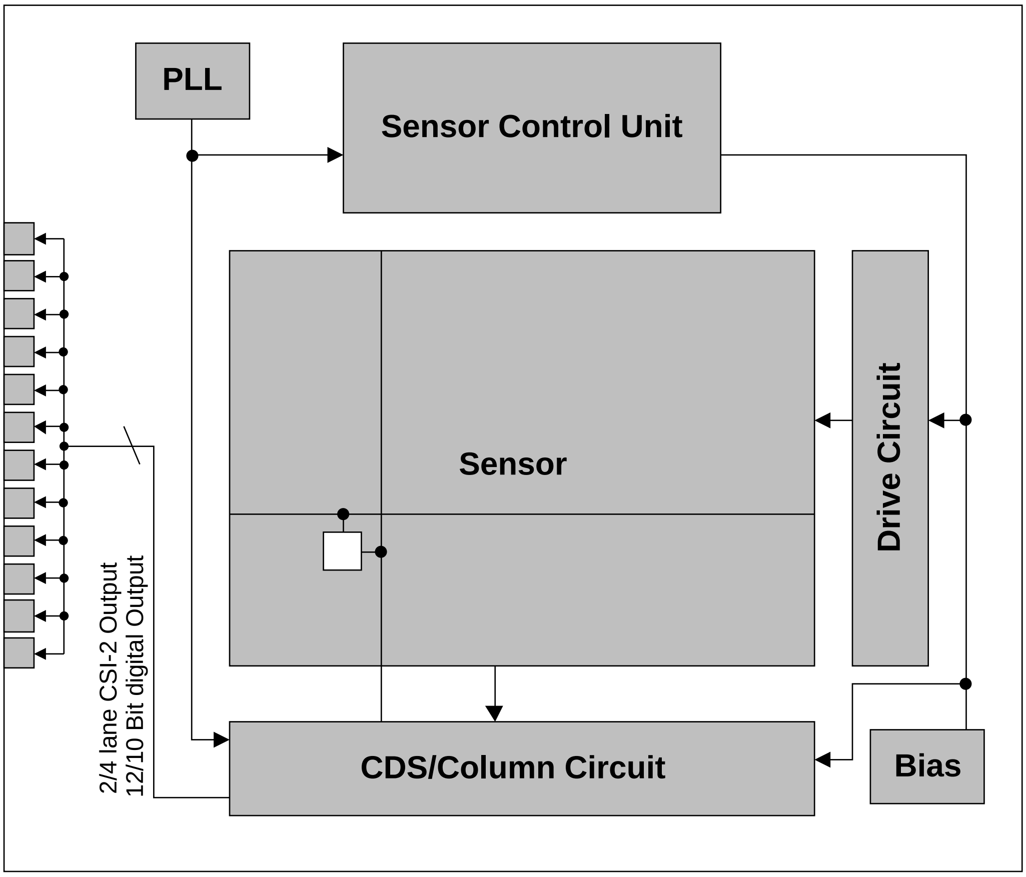
Pixel Arrangement



* Reference pin number is consecutive numbering of package pin array.
See the Pin Configuration for the number of each pin.

Pixel Arrangement (Top View)

Block Diagram and Pin Configuration



Block Diagram

	10	9	8	7	6	5	4	3	2	1
A	(GND) NC	VDDLCN	VDDLSC	SCL	TEST2	XMASTER	VDDLSC	VDDLCN	VSSLCB	(GND) NC
B	VSSLCN	VSSLCN	VSSLSC	(GND) NC	SLAMODE	TENABLE	VSSLSC	(GND) NC	VSSLSC	VDDLSC
C	VDDHPX	VSSHPX	VDDHCM	(GND) NC	(GND) NC	VDDHCM	VSSHPX	VDDHPX	VSSLPL1	VDDLPL1
D	VBGR	(GND) NC	(GND) NC					(GND) NC	XHS	TOUT
E	VDDHDA	VSSHDA	(GND) NC					VDDHCP	XVS	VDDLSC
F	VDDHPX	VSSHPX	(GND) NC					VSSHCP	VSSLSC	VDDMIO
G	ASMON	VDDSUB	VDDLIF	VDDLIF	VDDLSC	VDDLPL2	VDDHPX	VRLS	XCLR	TEST1
H	(GND) NC	VSSLSC	VSSLIF	VSSLIF	VSSLSC	VSSLPL2	VSSHPX	VRLT	(GND) NC	SDA
J	VDDLSC	DMOP4	DMOP2	DMCKP	DMOP1	DMOP3	VSSLPL3	VDDMIO	VSSLSC	(GND) NC
K	(GND) NC	DMOM4	DMOM2	DMCKM	DMOM1	DMOM3	VDDLPL3	INCK	VDDLSC	(GND) NC

*The N.C. pin can be connected to GND.

Pin Configuration (Bottom View)

Pin Description

No.	Pin No	I/O	A/D	Symbol	Description	Remarks
1	A1	—	—	N.C.	—	GND connectable
2	A2	GND	D	VSSLCB	1.2 V GND	
3	A3	Power	D	VDDLCN	1.2 V power supply	
4	A4	Power	D	VDDLSC	1.2 V power supply	
5	A5	I	D	XMASTER	Master / Slave selection	High: Slave mode Low: Master mode
6	A6	I	D	TEST2	—	Connect to 1.8V power supply
7	A7	I	D	SCL	Serial clock input	I^2C: SCL pin
8	A8	Power	D	VDDLSC	1.2 V power supply	
9	A9	Power	D	VDDLCN	1.2 V power supply	
10	A10	—	—	N.C.	—	GND connectable
11	B1	Power	D	VDDLSC	1.2 V power supply	
12	B2	GND	D	VSSLSC	1.2 V GND	
13	B3	—	—	N.C.	—	GND connectable
14	B4	GND	D	VSSLSC	1.2 V GND	
15	B5	I	D	TENABLE	TEST Enable	OPEN
16	B6	I	D	SLAMODE	Reference pin	Select slave address
17	B7	—	—	N.C.	—	GND connectable
18	B8	GND	D	VSSLSC	1.2 V GND	
19	B9	GND	D	VSSLCN	1.2 V GND	
20	B10	GND	D	VSSLCN	1.2V GND	
21	C1	Power	A	VDDLPL1	1.2 V power supply	
22	C2	GND	A	VSSLPL1	1.2 V GND	
23	C3	Power	A	VDDHPX	2.9 V power supply	
24	C4	GND	A	VSSHPX	2.9 V GND	
25	C5	Power	A	VDDHCM	2.9 V power supply	
26	C6	—	—	N.C.	—	GND connectable
27	C7	—	—	N.C.	—	GND connectable
28	C8	Power	A	VDDHCM	2.9 V power supply	
29	C9	GND	A	VSSHPX	2.9 V GND	
30	C10	Power	A	VDDHPX	2.9 V power supply	
31	D1	O	D	TOUT	TEST output pin	OPEN
32	D2	I/O	D	XHS	Horizontal sync signal	
33	D3	—	—	N.C.	—	GND connectable
34	D8	—	—	N.C.	—	GND connectable
35	D9	—	—	N.C.	—	GND connectable
36	D10	O	A	VBGR	Capacitor connection	
37	E1	Power	D	VDDLSC	1.2 V power supply	

No.	Pin No	I/O	A/D	Symbol	Description	Remarks
38	E2	I/O	D	XVS	Vertical sync signal	
39	E3	Power	A	VDDHCP	2.9 V power supply	
40	E8	—	—	N.C.	—	GND connectable
41	E9	GND	A	VSSHDA	2.9 V GND	
42	E10	Power	A	VDDHDA	2.9 V power supply	
43	F1	Power	D	VDDMIO	1.8 V power supply	
44	F2	GND	D	VSSLSC	1.2 V GND	
45	F3	GND	A	VSSHCP	2.9 V GND	
46	F8	—	—	N.C.	—	GND connectable
47	F9	GND	A	VSSHPX	2.9 V GND	
48	F10	Power	A	VDDHPX	2.9 V power supply	
49	G1	O	D	TEST1	Test output	OPEN
50	G2	I	D	XCLR	System clear	High: Normal Low: Clear
51	G3	O	A	VRLS	Capacitor connection	
52	G4	Power	A	VDDHPX	2.9 V power supply	
53	G5	Power	A	VDDLPL2	1.2 V power supply	
54	G6	Power	D	VDDLSC	1.2 V power supply	
55	G7	Power	D	VDDLIF	1.2 V power supply	
56	G8	Power	D	VDDLIF	1.2 V power supply	
57	G9	Power	A	VDDSUB	2.9 V power supply	
58	G10	Power	A	ASMON	Reference pin	OPEN
59	H1	I/O	D	SDA	Serialdata communication	I^2C: SDA pin
60	H2	—	—	N.C.	—	GND connectable
61	H3	O	A	VRLT	Capacitor connection	
62	H4	GND	A	VSSHPX	2.9 V GND	
63	H5	GND	A	VSSLPL2	1.2 V GND	
64	H6	GND	D	VSSLSC	1.2 V GND	
65	H7	GND	D	VSSLIF	1.2 V GND	
66	H8	GND	D	VSSLIF	1.2 V GND	
67	H9	GND	D	VSSLSC	1.2 V GND	
68	H10	—	—	N.C.	—	GND connectable
69	J1	—	—	N.C.	—	GND connectable
70	J2	GND	D	VSSLSC	1.2 V GND	
71	J3	Power	D	VDDMIO	1.8 V power supply	
72	J4	GND	A	VSSLPL3	1.2 V GND	
73	J5	O	D	DMOP3	CSI-2 output	
74	J6	O	D	DMOP1	CSI-2 output	
75	J7	O	D	DMCKP	CSI-2 output	
76	J8	O	D	DMOP2	CSI-2 output	
77	J9	O	D	DMOP4	CSI-2 output	
78	J10	Power	D	VDDLSC	1.2 V power supply	

No.	Pin No	I/O	A/D	Symbol	Description	Remarks
79	K1	—	—	N.C.	—	GND connectable
80	K2	Power	D	VDDLSC	1.2 V power supply	
81	K3	I	D	INCK	Master clock input	
82	K4	Power	A	VDDLPL3	1.2 V power supply	
83	K5	O	D	DMOM3	CSI-2 output	
84	K6	O	D	DMOM1	CSI-2 output	
85	K7	O	D	DMCKM	CSI-2 output	
86	K8	O	D	DMOM2	CSI-2 output	
87	K9	O	D	DMOM4	CSI-2 output	
88	K10	—	—	N.C.	—	GND connectable

Electrical Characteristics

DC Characteristics

Item		Pins	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Analog1	VDDSUB VDDHCP VDDHDA VDDHCM	AV_{DD1}		2.80	2.90	3.00	V
	Analog2	VDDHPX	AV_{DD2}		2.80	2.90	3.00	V
	Interface	VDDMIO	OV_{DD}		1.70	1.80	1.90	V
	Digital1	VDDLCN VDDLSC VDDLPL1	DV_{DD1}		1.10	1.20	1.30	V
	Digital2	VDDLPL2 VDDLPL3 VDDLIF	DV_{DD2}		1.10	1.20	1.30	V
Digital input voltage		XHS XVS XCLR INCK XMASTER SLAMODE SCL SDA TEST2	VIH	XVS / XHS Slave Mode	$0.8OV_{DD}$	—	—	V
			VIL		—	—	$0.2OV_{DD}$	V
		XHS XVS TOUT TEST1	VOH	XVS / XHS Master Mode	OV_{DD}-0.4	—	—	V
			VOL		—	—	0.4	V

Current Consumption

Item	Symbol	Typ.		Max.		Unit
		Standard luminous intensity	Saturated luminous intensity	Standard luminous intensity	Saturated luminous intensity	
Operating current MIPI CSI-2 / 4 Lane 10 bit, 60 frame/s All-pixel scan mode	I_{AVDD1}	TBD	TBD	TBD	TBD	mA
	I_{AVDD2}	TBD	TBD	TBD	TBD	mA
	I_{OVDD}	TBD	TBD	TBD	TBD	mA
	I_{DVDD1}	TBD	TBD	TBD	TBD	mA
	I_{DVDD2}	TBD	TBD	TBD	TBD	mA
Standby current	I_{AVDD1_STB}	TBD		TBD		mA
	I_{AVDD2_STB}	TBD		TBD		mA
	I_{OVDD_STB}	TBD		TBD		mA
	I_{DVDD1_STB}	TBD		TBD		mA
	I_{DVDD2_STB}	TBD		TBD		mA

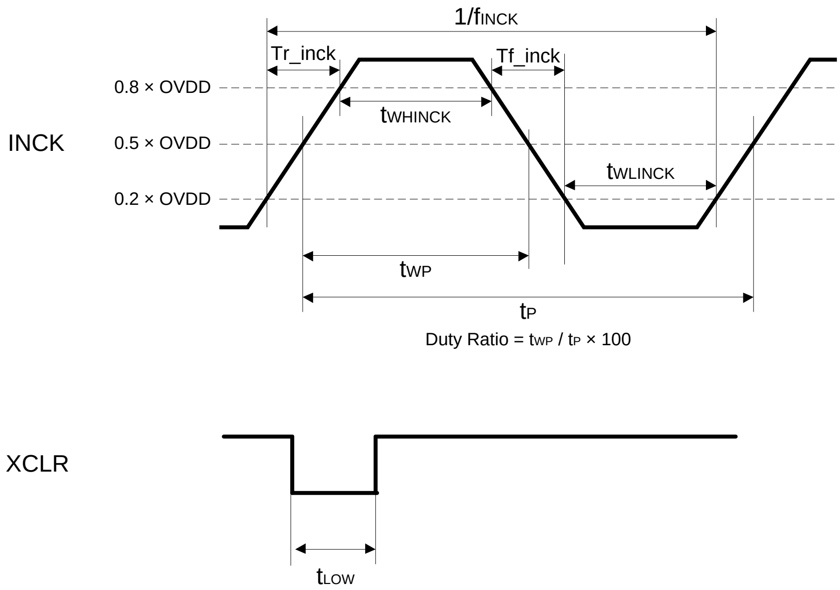
Operating current: (Typ.) Supply voltage 2.90 V / 1.8 V / 1.2 V, Tj = 25 °C
(Max.) Supply voltage 3.00 V / 1.9 V / 1.3 V, Tj = 60 °C, worst state of internal circuit operating current consumption,

Standby: (Max.) Supply voltage 3.00 V / 1.9 V / 1.3 V, Tj = 60 °C, INCK: 0 V, light-obstructed state.

Standard luminous intensity: luminous intensity at 1/3 of the sensor saturated
Saturated luminous intensity: luminous intensity when the sensor is saturated.

AC Characteristics

Master Clock Waveform (INCK)



INCK 37.125MHz, 74.25MHz

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK clock duty	—	45.0	50.0	55.0	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	80 % to 20 %
XCLR Low level pulse width	t_{LOW}	100	—	—	ns	

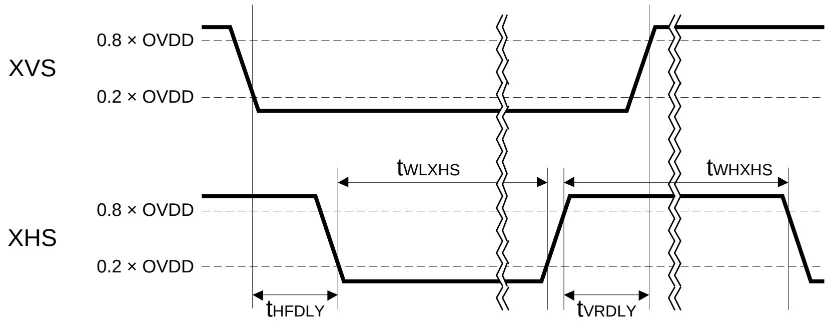
*The INCK fluctuation affects the frame rate.

INCK 6～27MHz

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	6	—	27	MHz	f_{INCK} = 6～27MHz
INCK Low level pulse width	t_{WLINCK}	5	—	—	ns	f_{INCK} = 6～27MHzz
INCK High level pulse width	t_{WHINCK}	5	—	—	ns	f_{INCK} = 6～27MHz
INCK clock duty	—	45.0	50.0	55.0	%	Define with 0.5 × OV_{DD}
INCK Rise time	Tr_inck	—	—	5	ns	20 % to 80 %
INCK Fall time	Tf_inck	—	—	5	ns	80 % to 20 %
XCLR Low level pulse width	t_{LOW}	100	—	—	ns	

*The INCK fluctuation affects the frame rate.

XVS / XHS Input Characteristics In Slave Mode (XMASTER pin = High)



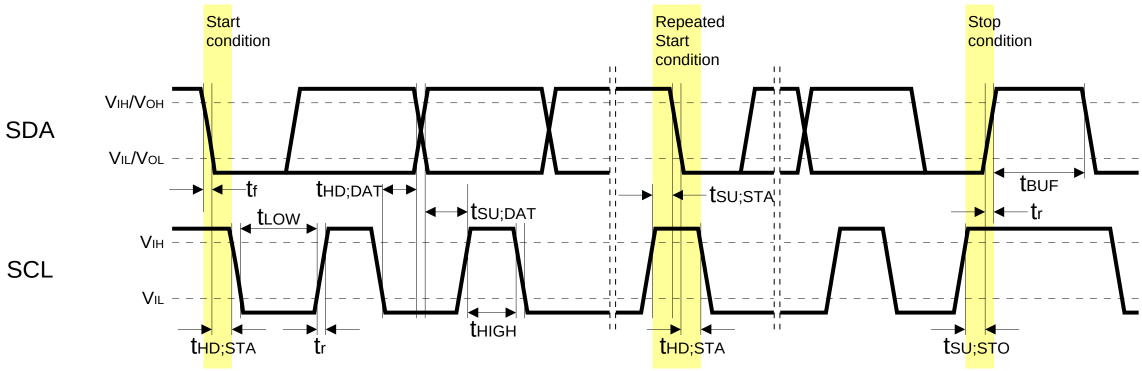
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	$4 / f_{INCK}$	—	—	ns	
XHS High level pulse width	t_{WHXHS}	$4 / f_{INCK}$	—	—	ns	
XVS - XHS fall width	t_{HFDLY}	$1 / f_{INCK}$	—	—	ns	
XHS - XVS rise width	t_{VRDLY}	$1 / f_{INCK}$	—	—	ns	

XVS / XHS Input Characteristics In Master Mode (XMASTER pin = Low)

* XVS and XHS cannot be used for the sync signal to pixels.
Be sure to detect sync code to detect the start of effective pixels in 1 line.
For the output waveforms in master mode, see the item of “Slave Mode and Master Mode”

Serial Communication

I²C



I²C Specification

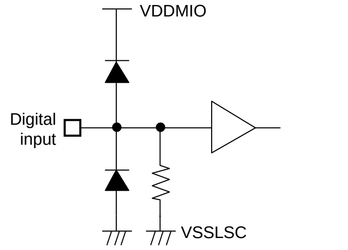
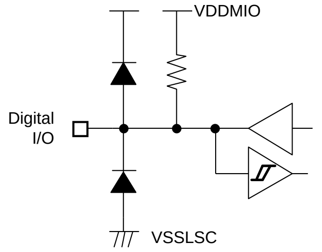
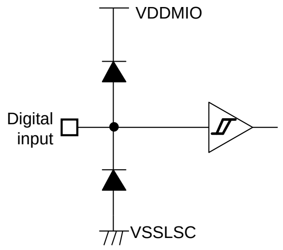
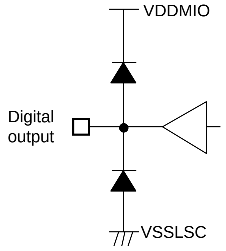
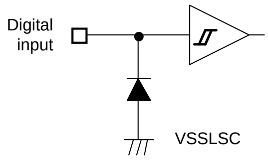
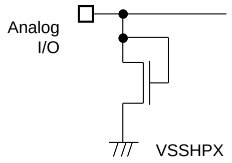
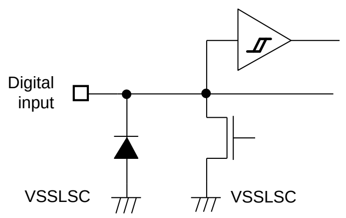
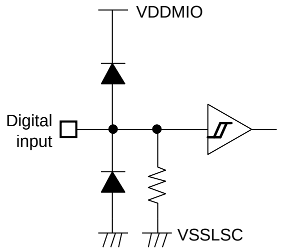
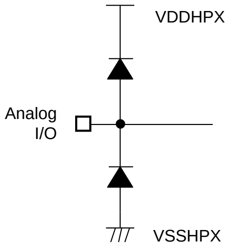
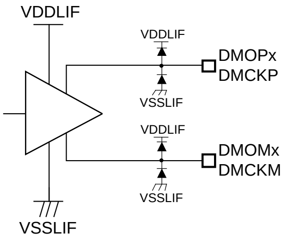
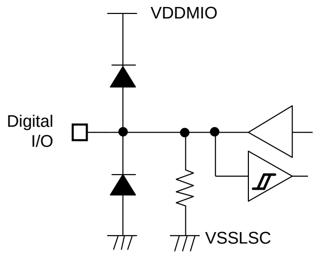
Item	Symbol	Min.	Typ.	Max.	Unit	条件
Low level input voltage	VIL	-0.3	—	$0.3 \times OV_{DD}$	V	
High level input voltage	VIH	$0.7 \times OV_{DD}$	—	1.9	V	
Low level input voltage	VOL	0	—	$0.2 \times OV_{DD}$	V	OVDD < 2 V, Sink 3 mA
High level input voltage	VOH	$0.8 \times OV_{DD}$	—	—	V	
Output fall time	tof	—	—	250	ns	Load 10 pF – 400 pF, $0.7 \times OV_{DD}$ – $0.3 \times OV_{DD}$
Input current	Ii	-10	—	10	µA	$0.1 \times OV_{DD}$ – $0.9 \times OV_{DD}$
Capacitance for SCK (SCL) /SDI (SDA)	Ci	—	—	10	pF	

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	µs
Low period of the SCL clock	t_{LOW}	1.3	—	—	µs
High period of the SCL clock	t_{HIGH}	0.6	—	—	µs
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	µs
Data hold time	$t_{HD;DAT}$	0	—	0.9	µs
Data set-up time	$t_{SU;DAT}$	100	—	—	ns
Rise time of both SDA and SCL signals	t_r	—	—	300	ns
Fall time of both SDA and SCL signals	t_f	—	—	300	ns
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	µs
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	µs

I/O Equivalent Circuit Diagram

□: External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
TENABLE		XVS XHS	
XMASTER TEST2		TOUT TEST1	
XCLR INCK		VRLS VRLT	
SDA SCL		SLAMODE	
VBGR ASMON		DMOPx DMOMx DMCKP DMCKM	
TOUT			

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics.)

TBD

Image Sensor Characteristics

(AV_{DD} = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, All-pixel scan mode, 12 bit 30 frame/s, Gain: 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		S	TBD	TBD	—	Digit (mV)	1	1/30 s storage 12 bit converted value HCG mode
Sensitivity ratio	R / G	RG	TBD	—	TBD	—	2	—
	B / G	BG	TBD	—	TBD	—		—
Saturation signal		Vsat	TBD	—	—	Digit (mV)	3	12 bit converted value LCG mode
Vertical line		VL			TBD	µV	5	12 bit converted value LCG mode

Note)

1. Converted value into mV using 1Digit = TBD mV for 12-bit output and 1Digit = TBD mV for 10-bit output.
2. The characteristics above apply to effective pixel area that is shown below.

Zone Definition

TBD

Image Sensor Characteristics Measurement Method

Measurement Conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr / Gb channel signal output or the R / B channel signal output of the measurement system.

Color Coding of Physical Pixel Array

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance - 30 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   Sg = (VGr + VGb) / 2 × 100/30 [mV]

2. Sensitivity ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr and Gb signal outputs to TBD mV, measure the R signal output (VR [mV]), the Gr and Gb signal outputs (VGr, VGb [mV]) and the B signal output (VB [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

   VG = (VGr + VGb) / 2
   RG = VR / VG
   BG = VB / VG

3. Saturation signa l
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, TBD mV, measure the average values of the Gr, Gb, R and B signal outputs.

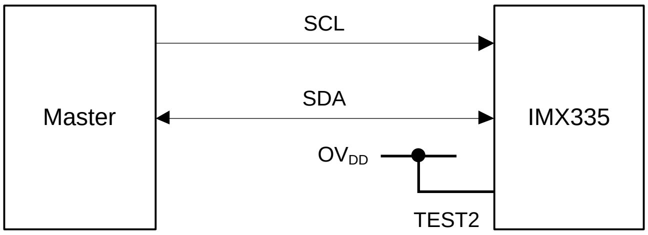
4. Vertical Line
   With the device junction temperature of 60 ˚C and the device in the light-obstructed state, calculates eachaverage output of Gr, Gb, R and B on respective columns. Calculates maximum value of difference with adjacent column on the same color (VL [µV]).

Setting Registers Using Serial Communication

This sensor can write and read the setting values of the various registers shown in the Register Map by I^2C communication. See the Register Map for the addresses and setting values to be set.

Description of Setting Registers (I^2C)

The serial data input order is MSB-first transfer. The table below shows the various data types and descriptions. Using SLAMODE pin , SLAVE address can be changed.



Pin connection of serial communication

SLAVE Address

SLAMODE pin	MSB							LSB
Low	0	0	1	1	0	1	0	R / W
High	0	0	1	0	0	0	0	R / W

* R/W is data direction bit

R / W

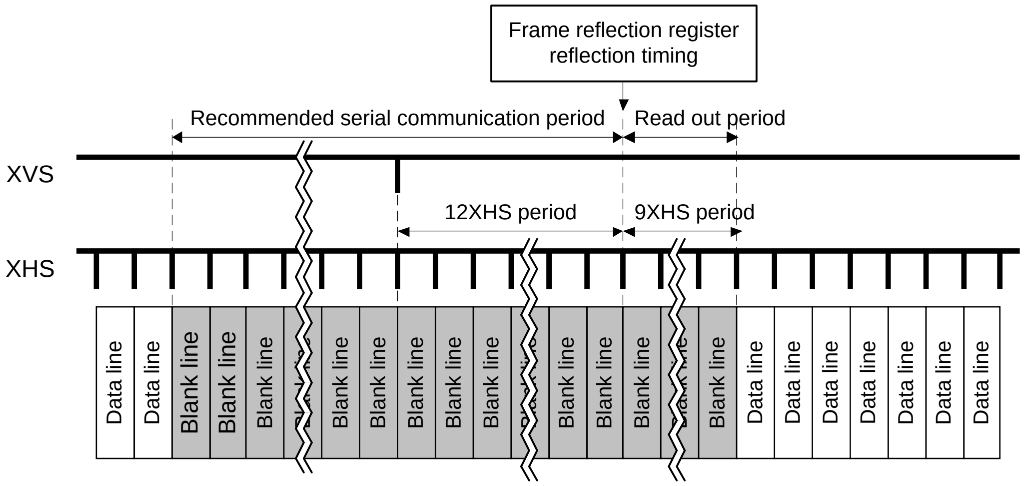
R / W bit	Data direction
0	Write (Master → Sensor)
1	Read (Sensor → Master)

I^2C pin description

Symbol	Pin No.	Remarks
SCL	A7	I^2C serial clock input
SDA	H1	I^2C serial data communication

Register Communication Timing (I^2C)

In I^2C communication system, communication can be performed during the falling edge of XVS to 12H. For the registers marked "V" in the item of Reflection timing, when the communication is performed in the communication period shown in the figure below they are reflected by frame reflection timing. For the registers noted “Immediately” in the item of Reflection timing, the settings are reflected when the communication is performed. (For the immediate reflection registers other than STANDBY, REGHOLD, XMSTA, SW_RESET, XVSOUTSEL [1:0] and XHSOUTSEL [1:0], set them in sensor standby state.) Using REG_HOLD function is recommended for register setting using I^2C communication. For REG_HOLD function, see “Register Transmission Setting” in “Description of Functions”.



Communication Protocol

I^{2}C serial communication supports a 16-bit register address and 8-bit data message type.

S	Slave Address [7:1]	R / W	A	Register Address [15:8]	A	Register Address [7:0]	A	DATA [7:0]	A / $\overline{A}$	P

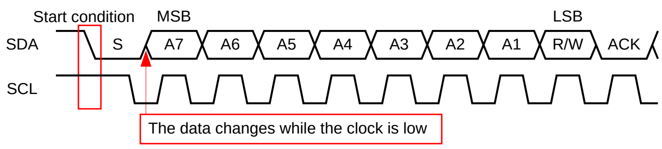
From Master to Slave (green)
From Slave to Master (white)
Direction depend on operation (orange)

S : Start Condition
Sr : Repeated Start Condition
P : Stop Condition
A : Acknowledge
$\overline{A}$: Negative Acknowledge

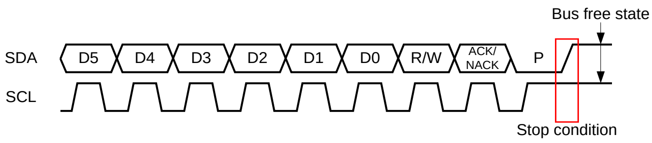
R/W=
0: Write (Master → Sensor)
1: Read (Sensor → Master)

Communication Protocol

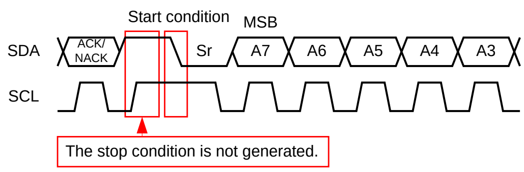
Data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / $\overline{A}$ (Negative Acknowledge) is transferred. Data (SDA) is transferred at the clock (SDL) cycle. SDA can change only while SCL is Low, so the SDA value must be held while SCL is High. The Start condition is defined by SDA changing from High to Low while SCL is High. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.



Start Condition

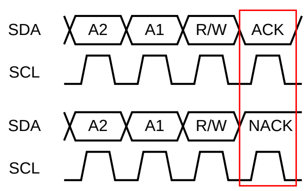


Stop Condition



Repeated Start Condition

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative Acknowledge and release (does not drive) SDA. When Negative Acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.



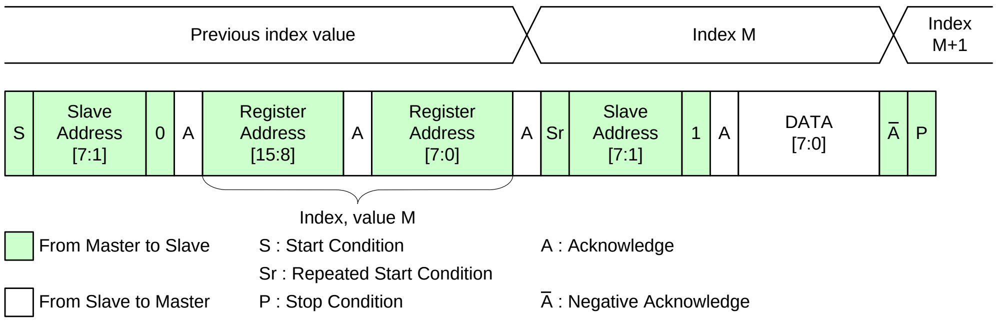
Acknowledge and Negative Acknowledge

Register Write and Read (I^2C)

This sensor corresponds to four reed modes and the two write modes.

Single Read from Random Location

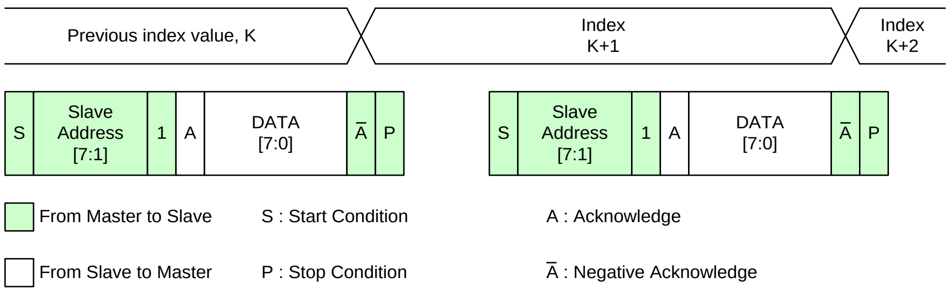
The sensor has an index function that indicates which address it is focusing on. In reading the data at an optional single address, the Master must set the index value to the address to be read. For this purpose it performs dummy write operation up to the register address. The upper level of the figure below shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the index address data on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication



Single Read from Random Location

Single Read from Current Location

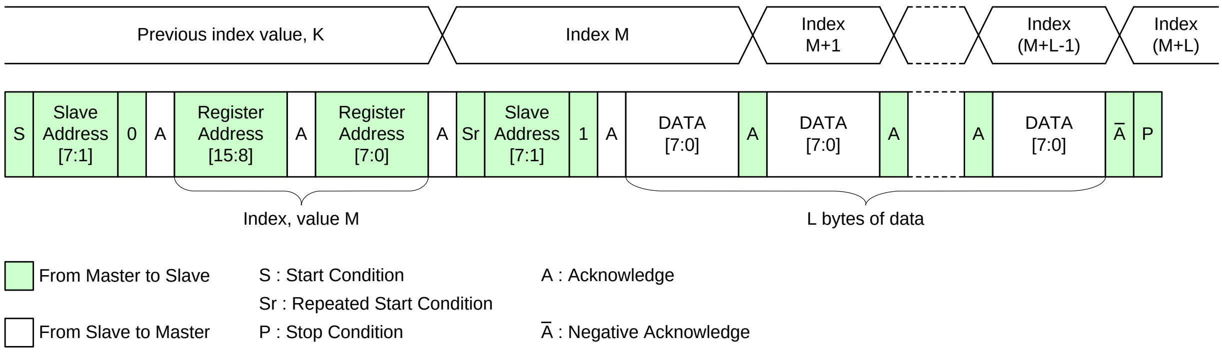
After the slave address is transmitted by a write request, that address is designated by the next communication and the index holds that value. In addition, when data read/write is performed, the index is incremented by the subsequent Acknowledge/Negative Acknowledge timing. When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after Acknowledge. After receiving the data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication, but the index value is incremented, so the data at the next address can be read by sending the slave address with a read request.



Single Read from Current Location

Sequential Read Starting from Random Location

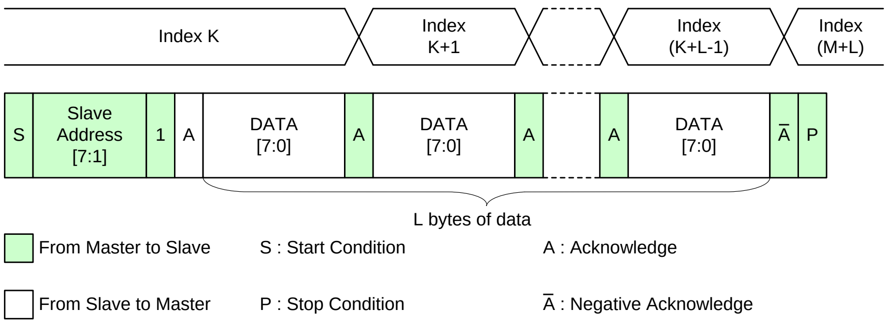
In reading data sequentially, which is starting from an optional address, the Master must set the index value to the start of the addresses to be read. For this purpose, dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the index address data on SDA. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Random Location

Sequential Read Starting from Current Location

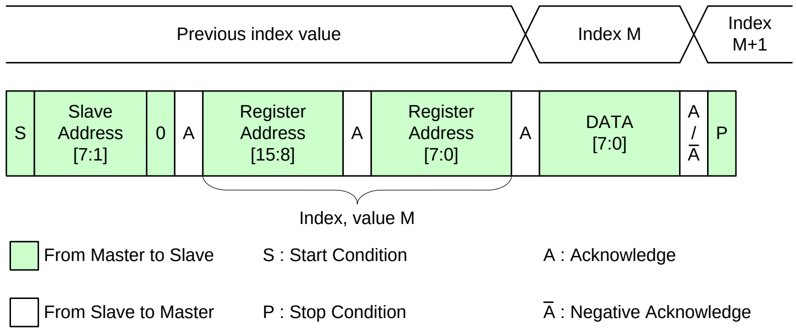
When the index value is known to indicate the address to be read, sending the slave address with a read request allows the data to be read immediately after the Acknowledge. When the Master outputs an Acknowledge after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Sequential Read Starting from Current Location

Single Write to Random Location

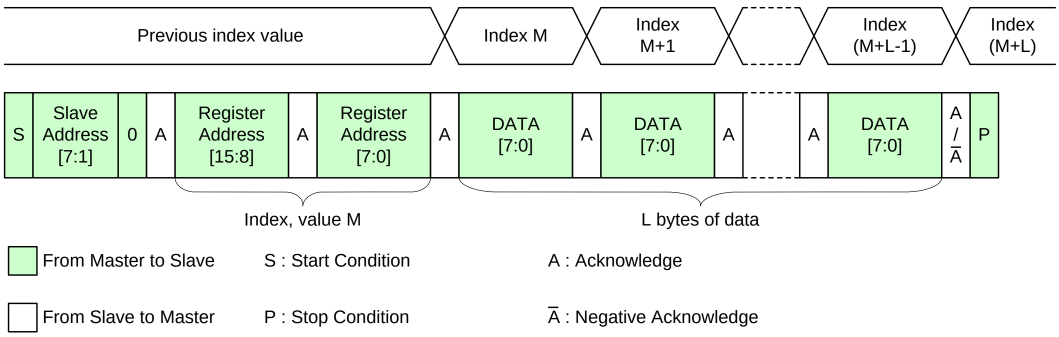
The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



Single Write to Random Location

Sequential Write Starting from Random Location

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



Sequential Write Starting from Random Location

Register Map

This sensor has a total of 2816 bytes (256 × 11) of registers, composed of registers with addresses 00h to FFh that correspond to address 30h to30Ah. Use the initial values for empty address. Some registers must be change from the initial values, so the sensor control side should be capable of setting 2816 bytes.

The values must be changed from the default value, so initial setting after reset is required after power-on. There are two different register reflection timing. Values are reflected immediately after writing to register noted as “Immediately”, or at the frame reflection register reflection timing described in the item of “Register Communication Timing” in the section of “Setting Registers with Serial Communication” for registers noted as “V” in the Reflection timing column of the Register Map. For the immediate reflection registers other than belows, set them in sensor standby state.

STANDBY
REGHOLD
XVSOUTSEL [1:0]
XHSOUTSEL [1:0]

Do not perform communication to addresses not listed in the Register Map. Doing so may result in operation errors. However, other registers that requires communication to address not listed above may be added, so addresses up to FFh should be supported for LSB address; 01h to 0Ah. (In I^2C communication, address; 3000h to 3AFFh)

* For the register that is writing " * " to the setting value in description (Indicated by red letter), change the value from the default value after the reset.

** In Gain setting only, it is reflected on the next frame which was settings.

(1) Registers corresponding to address = 30**h.

Address	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
3000h	0	STANDBY	Standby 0: Operating 1: Standby	1h	01h	Immediately
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3001h	0	REGHOLD	Register hold (Function not to update V reflection register) 0: Invalid 1: Valid	0h	00h	Immediately
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3002h	0	XMSTA	Setting of master mode operation 0: Master mode operation start 1: Master mode operation stop	1h	01h	Immediately
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3003h	[7:0]	—	Fixed to “0h”	0h	0h	—
3004h ~ 300Bh	[7:0]	—	Reserved	—	—	—
300Ch	0 1 2 3 4 5 6 7	BCWAIT_TIME [7:0]	LSB The value is set according to INCK INCK = 74.25 MHz: B6h INCK = 37.125 MHz: 5Bh INCK = 24 MHz: 3Bh INCK = 18 MHz: 2Dh INCK = 12 MHz: 1Eh INCK = 6 MHz: 0Fh MSB	B6h	B6h	Immediately
300Dh	0 1 2 3 4 5 6 7	CPWAIT_TIME [7:0]	LSB The value is set according to INCK INCK = 74.25 MHz: 7Fh INCK = 37.125 MHz: 40h INCK = 24 MHz: 2Ah INCK = 18 MHz: 1Fh INCK = 12 MHz: 15h INCK = 6 MHz: 0Bh MSB	7Fh	7Fh	Immediately

Address	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
300Eh ~ 3017h	[7:0]	—	Reserved	—	—	—
3018h	0	WINMODE [3:0]	Window mode setting 0: All-pixel scan mode 1: Horizontal/Vertical 2/2-line binning 4: Window cropping mode Others: Setting prohibited	0h	00h	V
	1					
	2					
	3					
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3019h ~ 302Bh	[7:0]	—	Reserved	—	—	—
302Ch	0	HTRIMMING_ START [11:0]	LSB In window cropping mode Start position (Horizontal direction)	030h	30h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
302Dh	0				00h	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
302Eh	0	HNUM [11:0]	LSB In window cropping mode Cropping sizes designation (Horizontal direction)	A38h	38h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
302Fh	0				0Ah	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset: By register	Default value after reset: By address	Reflection timing
3030h	0	VMAX [19:0]	LSB	01194h	94h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7		When sensor master mode vertical span setting.			
3031h	0				11h	
	1		For details, see the item of “Slave Mode and Master Mode” In the section of “Description of Various Functions”			
	2					
	3					
	4					
	5					
	6					
	7					
3032h	0				00h	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3033h	[7:0]	—	Fixed to “0h”	00h	00h	—
3034h	0	HMAX [15:0]	LSB	0226h	26h	V
	1					
	2					
	3					
	4					
	5		When sensor master mode horizontal span setting.			
	6					
	7					
3035h	0		For details, see the item of “Slave Mode and Master Mode” In the section of “Description of Various Functions”		02h	
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			
3036h ~ 304Bh	[7:0]	—	Reserved	—	—	—
304Ch	0	OPB_SIZE_V [5:0]	LSB	14h	14h	V
	1					
	2		Vertical direction OB width setting.			
	3					
	4					
	5		MSB			
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
304Dh	[7:0]	—	Reserved	—	—	—

Address	bit	Register name	Description	Default value after reset: By register	Default value after reset: By address	Reflection timing
304Eh	0	HREVERSE	Horizontal direction Readout inversion control 0: Normal 1: Inverted	0h	00h	V
	1		Fixed to “0h”	0h		—
	2		Fixed to “0h”	0h		—
	3		Fixed to “0h”	0h		—
	4		Fixed to “0h”	0h		—
	5		Fixed to “0h”	0h		—
	6		Fixed to “0h”	0h		—
	7		Fixed to “0h”	0h		—
304Fh	0	VREVERSE	Vertical direction 0: Normal 1: Inverted	0h	00h	V
	1		Fixed to “0h”	0h		—
	2		Fixed to “0h”	0h		—
	3		Fixed to “0h”	0h		—
	4		Fixed to “0h”	0h		—
	5		Fixed to “0h”	0h		—
	6		Fixed to “0h”	0h		—
	7		Fixed to “0h”	0h		—
3050h	0	ADBIT	ADconversion bits setting 0: AD10bit 1: AD12bit	1h	01h	Immediately
	1		Fixed to “0h”	0h		—
	2		Fixed to “0h”	0h		—
	3		Fixed to “0h”	0h		—
	4		Fixed to “0h”	0h		—
	5		Fixed to “0h”	0h		—
	6		Fixed to “0h”	0h		—
	7		Fixed to “0h”	0h		—
3051h ~ 3055h	[7:0]	—	Reserved	—	—	—
3056h	0	Y_OUT_SIZE [12:0]	LSB	7ACh	ACh	V
	1					
	2					
	3					
	4					
	5					
	6		Set the number of effective pixel lines			
	7					
3057h	0				07h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
3058h	0	SHR0 [19:0]	LSB	00009h	09h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3059h	0		Storage time adhustment Designated in line units.		00h	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
305Ah	0				00h	
	1					
	2					
	3		MSB			
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
305Bh ~ 3071h	[7:0]	—	Reserved	—	—	—
3072h	0	AREA2_WIDTH_1 [12:0]	LSB	0028h	28h	V
	1					
	2					
	3					
	4					
	5		In window cropping mode OB cropping size designation (Vertical direction)			
	6					
	7					
3073h	0				00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—

Address	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
3074h	0	AREA3_ST_ADR_1 [12:0]	LSB	00B0h	B0h	V
	1					
	2					
	3					
	4		In window cropping mode			
	5		Designation of upper left coordinate for cropping position			
	6		(Vertical position)			
	7					
3075h	0				00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3076h	0	AREA3_WIDTH_1 [12:0]	LSB	0F58h	58h	V
	1					
	2					
	3					
	4					
	5		In window cropping mode			
	6		Cropping size designation			
	7		(Vertical direction)			
3077h	0				0Fh	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3078h ~ 30C5h	[7:0]	—	Reserved	—	—	—

Address	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
30C6h	0	BLACK_OFSET_ADR [12:0]	LSB	0000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6		In window cropping mode			
	7					
30C7h	0				00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
30C8h ~ 30CDh	[7:0]	—	Reserved	—	—	—
30CEh	0	UNRD_LINE_MAX [12:0]	LSB	0000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6		In window cropping mode			
	7					
30CFh	0				00h	
	1					
	2					
	3					
	4		MSB			
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
30D0h ~ 30D7h	[7:0]	—	Reserved	—	—	—
30D8h	0	UNREAD_ED_ADR [12:0]	LSB	104Ch	4Ch	V
	1					
	2					
	3					
	4					
	5					
	6		In window cropping mode			
	7					
30D9h	0				10h	
	1					
	2					
	3					
	4		MSB	0h		
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
30DAh ~ 30E7h	[7:0]	—	Reserved	—	—	—
30E8h	0	GAIN [10:0]	LSB Gain setting (0.0dB to TBDdB / 0.3dB step) MSB	000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
30E9h	0				00h	
	1					
	2					
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
30EAh ~ 30FFh	[7:0]	—	Reserved	—	—	—

(2) Registers corresponding to address = 31**h.

Address	bit	Register name	Description	Default value after reset: By register	Default value after reset: By address	Reflection timing
3100h ~ 314Bh	[7:0] ~ [7:0]	—	Reserved	—	—	—
314Ch	0	INCKSEL1 [8:0]	LSB The value is set according to INCK. Refer to page 73. MSB	080h	80h	Immediately
	1					
	2					
	3					
	4					
	5					
	6					
	7					
314Dh	0				00h	
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
314Eh ~ 3159h	[7:0] ~ [7:0]	—	Reserved	—	—	—
315Ah	0	INCKSEL2 [1:0]	The value is set according to INCK. INCK = 74.25 MHz: 3h INCK = 37.125 MHz: 2h INCK = 24 MHz: 2h INCK = 18 MHz: 1h INCK = 12 MHz: 1h INCK = 6 MHz: 0h	3h	03h	Immediately
	1					
	2	PLL_IF_GC [3:2]	The value is set according to Data rate 1188Mbps: 0h 891Mbps: 1h	0h		—
	3					—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
315Bh ~ 3167h	[7:0] ~ [7:0]	—	Reserved	—	—	—
3168h	0	INCKSEL3 [7:0]	LSB The value is set according to INCK. INCK = 74.25 MHz: 68h INCK = 37.125 MHz: 68h INCK = 24 MHz: A0h INCK = 18 MHz: 6Bh INCK = 12 MHz: A0h INCK = 6 MHz: A0h MSB	68h	68h	Immediately
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3169h	[7:0]	—	Reserved	—	—	—

Address	bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
316Ah	0	INCKSEL4 [1:0]	The value is set according to INCK. INCK = 74.25 MHz: 3h INCK = 37.125 MHz: 2h INCK = 24 MHz: 2h INCK = 18 MHz: 1h INCK = 12 MHz: 1h INCK = 6 MHz: 0h	3h	7F	Immediately
	1					
	2	—	Fixed to “1h”	1h		
	3	—	Fixed to “1h”	1h		
	4	—	Fixed to “1h”	1h		
	5	—	Fixed to “1h”	1h		
	6	—	Fixed to “1h”	1h		
	7	—	Fixed to “0h”	0h		
316Bh ~ 3198h	[7:0] ~ [7:0]	—	Reserved	—	—	—
3199h	0	—	Fixed to “0h”	0h	00h	Immediately
	1	—	Fixed to “0h”	0h		
	2	—	Fixed to “0h”	0h		
	3	—	Fixed to “0h”	0h		
	4	HADD	Mode setting 0: All-pixel scan mode 1: Horizontal/Vertical 2/2-line binning	0h		
	5	VADD		0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
319Ah ~ 319Ch	[7:0] ~ [7:0]	—	Reserved	—	—	—
319Dh	0	MDBIT	Number of output bit setting 0: 10 bit 1: 12bit	1h	01h	V
	1	—	Fixed to “0h”	0h		
	2	—	Fixed to “0h”	0h		
	3	—	Fixed to “0h”	0h		
	4	—	Fixed to “0h”	0h		
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
319Eh	0	SYS_MODE	I/F mode change 1: 1188Mbps 2: 891Mbps Others: Setting prohibited	1h	01h	Immediately
	1	—	Fixed to “0h”	0h		
	2	—	Fixed to “0h”	0h		
	3	—	Fixed to “0h”	0h		
	4	—	Fixed to “0h”	0h		
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
319Fh	[7:0]	—	Reserved	—	—	—

Address	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
31A0h	0 1	XVSOUTSEL [1:0]	XVS pin setting in master mode 0: Fixed to High 2: VSYNC output Others: Setting prohibited	2h	2Ah	Immediately
	2 3	XHSOUTSEL [1:0]	XHS pin setting in master mode 0: Fixed to High 2: HSYNC output Others: Setting prohibited	2h		
	4	—	Fixed to "0h"	0h		—
	5	—	Fixed to "1h"	1h		—
	6	—	Fixed to "0h"	0h		—
	7	—	Fixed to "0h"	0h		—
31A1h ~ 31D3h	[7:0] ~ [7:0]	—	Reserved	—	—	—
31D4h	0	—	Fixed to "0h"	0h	00h	—
	1	—	Fixed to "0h"	0h		—
	2	—	Fixed to "0h"	0h		—
	3	—	Fixed to "0h"	0h		—
	4 5	XVSLNG [1:0]	XVS pulse width setting in master mode. 0: 1H 1: 2H 2: 4H 3: 8H	0h		Immediately
	6	—	Fixed to "0h"	0h		—
	7	—	Fixed to "0h"	0h		—
31D5h	0	—	Fixed to "0h"	0h	00h	—
	1	—	Fixed to "0h"	0h		—
	2	—	Fixed to "0h"	0h		—
	3	—	Fixed to "0h"	0h		—
	4 5	XHSLNG [1:0]	XHS pulse width setting in master mode. 0: 16clock 1: 32clock 2: 64clock 3: 128clock	0h		Immediately
	6	—	Fixed to "0h"	0h		—
	7	—	Fixed to "0h"	0h		—
31D6h ~ 31FFh	[7:0] ~ [7:0]	—	Reserved	—	—	—

(3) Registers corresponding to address = 33**h.

Address	bit	Register name	Description	Default value after reset: By register	Default value after reset: By address	Reflection timing
3300h	0	TCYCLE [1:0]	Mode setting 0: All-pixel scan mode 1: Horizontal/Vertical 2/2-line binning	0h	00h	Immediately
	1			0h		
	2	—	Fixed to “0h”	0h		
	3	—	Fixed to “0h”	0h		
	4	—	Fixed to “0h”	0h		
	5	—	Fixed to “0h”	0h		
	6	—	Fixed to “0h”	0h		
	7	—	Fixed to “0h”	0h		
3301h	[7:0]	—	Reserved	—	—	—
3302h	0	BLKLEVEL [9:0]	LSB Black level offset balue setting 10-bit readout mode: 1digit/1h 12-bit readout mode: 4digit/1h MSB	032h	32h	Immediately
	1					
	2					
	3					
	4					
	5					
	6					
	7					
3303h	0				00h	
	1					
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3304h ~ 33FFh	[7:0] ~ [7:0]	—	Reserved	—	—	—

(4) Registers corresponding to address = 34**h.

Address	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection timing
3400h ~ 341Bh	[7:0] ~ [7:0]	—	Reserved	—	—	—
341Ch	0	ADBIT1 [8:0]	LSB The value is set according to AD Conversion bits 10-bit : 1FFh 12-bit : 47h MSB	047h	47h	Immediately
	1					
	2					
	3					
	4					
	5					
	6					
	7					
341Dh	0				00h	
	1	—	Fixed to “0h”	0h		—
	2	—	Fixed to “0h”	0h		—
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
341Eh ~ 34FFh	[7:0] ~ [7:0]	—	Reserved	—	—	—

(5) Registers corresponding to address = 3A**h.

Address	bit	Register name	Description	Default value after reset By register	Default value after reset By address	Reflection ticiming
3A00h	[7:0]	—	Reserved	—	—	—
3A01h	0	LANEMODE [2:0]	Output interface selection 1: CSI-2 2lane 3: CSI-2 4lane Othears: Setting prohibited	03h	03h	Immediately
	1					
	2					
	3	—	Fixed to “0h”	0h		—
	4	—	Fixed to “0h”	0h		—
	5	—	Fixed to “0h”	0h		—
	6	—	Fixed to “0h”	0h		—
	7	—	Fixed to “0h”	0h		—
3A02h ~ 3A17h	[7:0] ~ [7:0]	—	Reserved	—	—	—
3A18h	[7:0]	TCLKPOST [9:0]	Global timing setting	08Fh	8Fh	Immediately
3A19h	[1:0]				00h	
	[7:2]	—	Fixed to “0h”	00h		—
3A1Ah	[7:0]	TCLKPREPARE [9:0]	Global timing setting	04Fh	4Fh	Immediately
3A1Bh	[1:0]				00h	
	[7:2]	—	Fixed to “0h”	00h		—
3A1Ch	[7:0]	TCLKTRAIL [9:0]	Global timing setting	047h	47h	Immediately
3A1Dh	[1:0]				00h	
	[7:2]	—	Fixed to “0h”	00h		—
3A1Eh	[7:0]	TCLKZERO [9:0]	Global timing setting	137h	37h	Immediately
3A1Fh	[1:0]				01h	
	[7:2]	—	Fixed to “0h”	00h		—
3A20h	[7:0]	THSPREPARE [9:0]	Global timing setting	04Fh	4Fh	Immediately
3A21h	[1:0]				00h	
	[7:2]	—	Fixed to “0h”	00h		—
3A22h	[7:0]	THSZERO [9:0]	Global timing setting	087h	87h	Immediately
3A23h	[1:0]				00h	
	[7:2]	—	Fixed to “0h”	00h		—
3A24h	[7:0]	THSTRAIL [9:0]	Global timing setting	04Fh	4Fh	Immediately
3A25h	[1:0]				00h	
	[7:2]	—	Fixed to “0h”	00h		—
3A24h	[7:0]	THSEXIT [9:0]	Global timing setting	07Fh	7Fh	Immediately
3A25h	[1:0]				00h	
	[7:2]	—	Fixed to “0h”	00h		—
3A28h	[7:0]	TLPX [9:0]	Global timing setting	03Fh	3Fh	Immediately
3A29h	[1:0]				00h	
	[7:2]	—	Fixed to “0h”	00h		—
3A30h ~ 3AFFh	[7:0] ~ [7:0]	—	Reserved	—	—	—

Readout Drive mode

The table below lists the operating modes available with this sensor. (N/A: Not supported mode)

Mode	INCK [MHz]	Recording Pixels H [pixels]	Recording Pixels V [lines]	AD conversion [bit]	Output bit width [bit]	Frame rate [frame/s]	Data rate CSI-2 [Mbps/Lane] 2 Lane	Data rate CSI-2 [Mbps/Lane] 4 Lane	1H period [μs] CSI-2 2 Lane	1H period [μs] CSI-2 4 Lane
All pixel	6-27 37.125 74.25	2592	1944	10	10	30 / 25	N/A	891	N/A	14.81
				10	10	30 / 25	1188	1188	14.81	14.81
				10	10	60 / 50	N/A	1188	N/A	7.41
				12	12	30 / 25	N/A	891/1188	N/A	14.81
2×2 binning	6-27 37.125 74.25	1296	972	10	12	30 / 25	891	891	29.63	29.63
				10	12	60 / 50	N/A	891	N/A	14.81
				10	12	30 / 25	1188	1188	29.63	29.63
				10	12	60 / 50	1188	1188	14.81	14.81

Image Data Output Format (CSI-2 output)

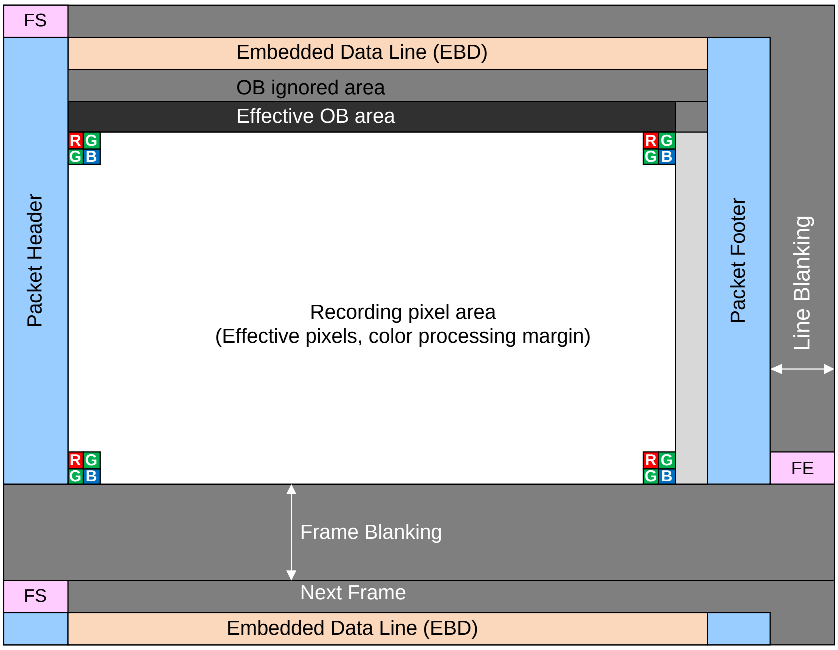
Frame Format

Each line of each image frame is output like the General Frame Format of CSI-2. The settings for each packet header are shown below.

DATA Type

Header [5:0]	Name	Setting register (I^2C)	Description
00h	Frame Start Code	N/A	FS
01h	Frame End Code	N/A	FE
10h	NULL	N/A	Invalid data
12h	Embedded Data	N/A	Embedded data
2Bh	RAW10	Address: 319Dh MDBIT [0]	0A0Ah
2Ch	RAW12		0C0Ch
37h	OB Data	N/A	Vertical OB line data

Frame Structure



Frame Structure of CSI-2 output

Embedded Data Line

The Embedded data line is output in a line following the sync code FS.

Embedded Data Format

Packet Header	A5h	Tag	Data	Tag	Data	Tag	Data	Tag	Data	Tag	Data	07h	07h	Packet Footer

RAW10

Packet Header	A5h	Tag	Data	Tag	55h	Data	Tag	Data	Tag	55h	Data	Tag	Data	07h	55h	Packet Footer

RAW12

Packet Header	A5h	Tag	55h	Data	Tag	55h	Data	Tag	55h	Data	Tag	55h	Data	07h	55h	Packet Footer

The end of the address and the register value is determined according to the tags embedded in the data.

Embedded Data Line Tag

Tag	Data Byte Description
00h	Illegal Tag. If found treat as end of Data.
07h	End of Data.
AAh	CCI Register Index MSB [15:8]
A5h	CCI Register Index LSB [7:0]
5Ah	Auto increment the CCI index after the data byte – valid data Data byte contains valid CCI register data.
55h	Auto increment the CCI index after the data byte – null data A CCI register does not exist for the current CCI index. The data byte value is the 07h.
FFh	Illegal Tag. If found treat as end of Data.

Specific output examples are shown below.

Outopput timing	bit	Transfer data	Description
E00 to E01	[7:0]	—	ignored
E02	[2:0]	—	ignored
	[3]	HREVERSE	
	[7:4]	—	ignored
E03 to E07	[7:0]	—	ignored
E08	[4:0]	—	ignored
	[5]	VREVERSE	
	[7:6]	—	ignored
E09	[7:0]	—	ignored
E10	[6:0]	—	ignored
	[7]	ADBIT	
E11	[7:0]	—	ignored
E12	[3:0]	—	ignored
	[5:4]	MDBIT	
	[7:6]	—	ignored
E13 to E14	[7:0]	—	ignored
E15	[7:0]	GAIN	
E16	[2:0]		
	[7:3]	—	ignored
E17 to E22	[7:0]	—	ignored
E23	[7:0]	SHR0	
E24	[7:0]		
E25	[3:0]		
	[7:4]	—	ignored
E26 to E52	[7:0]	—	ignored
E53	[7:0]	BLKLEVEL	
E54	[1:0]		
	[7:2]	—	ignored
E55 to E191	[7:0]	—	ignored

Image Data Output Format

All-pixel scan mode

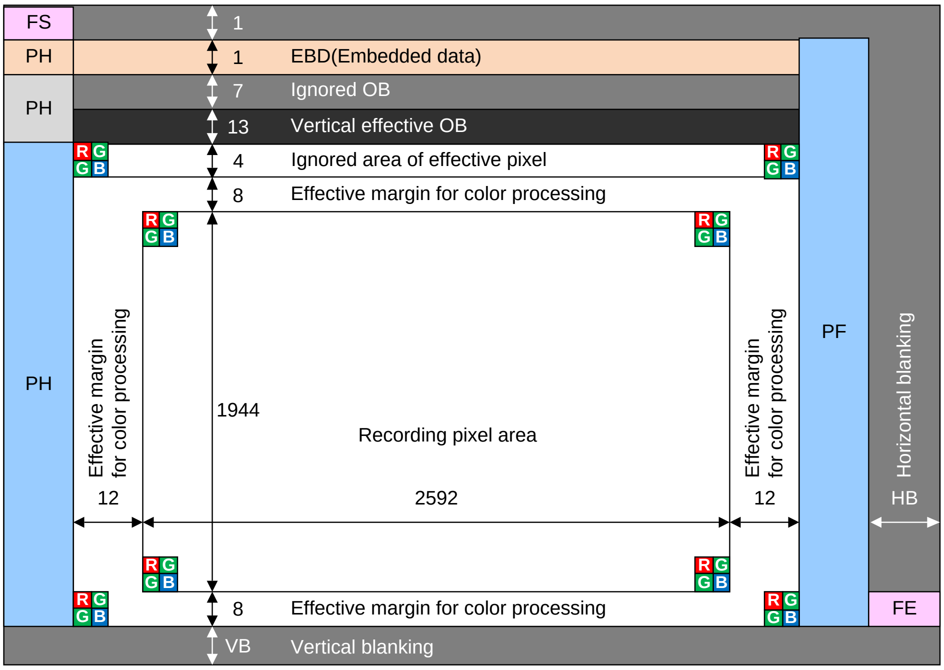
List of Setting Register

Address	bit	Register Name	Initial Value	CSI-2 serial						Remarks
				2 lane	4 lane					
				30 / 25 [frame /s]	30 / 25 [frame /s]	30 / 25 [frame /s]	60 /50 [frame /s]	30 /25 [frame /s]	30 / 25 [frame /s]	
AD Conversion				10	10	10	10	12	12	
Output bit width				10	10	10	10	12	12	
Data rate				1188	891	1188	1188	891	1188	
3018h	[3:0]	WINMODE	0h	0h						
3030h	[7:0]	VMAX	1194h	1194h						25 /30 / 50 / 60 [frame/s]
3031h	[7:0]									
3032h	[3:0]									
3034h	[7:0]	HMAX	0226h	0226h / 0294h	0226h / 0294h	0226h / 0294h	0113h / 014Ah	0226h / 0294h	0226h / 0294h	30 / 60[frame/ s] 25 / 50[frame/ s]
3035h	[7:0]									
304Ch	[5:0]	OPB_SIZE_V	14h	14h						
304Eh	[7:0]	HREVERSE	00h	00h / 01h						0: Normal, 1: Inverted
304Fh	[7:0]	VREVERSE	00h	00h / 01h						0: Normal 1: Inverted
3050h	[7:0]	ADBIT	01h	00h / 01h						0: 10 bit, 1: 12 bitt
3056h	[7:0]	Y_OUT_SIZE	7ACh	7ACh						
3057h	[7:0]									
3072h	[7:0]	AREA2_WIDTH_1	0028h	0028h						
3073h	[4:0]									
3074h	[7:0]	AREA3_ST_ ADR_1	00B0h	Vertical read out Normal：00B0h , Inverted：1010h						
3075h	[4:0]									
3076h	[7:0]	AREA3_WIDTH_1	0F58h	0F58h						
3077h	[4:0]									
314Ch	[7:0]	INCKSEL1	080h	Set according to INCK Refer to page 73						
314Dh	[0]									
315Ah	[1:0]	INCKSEL2	3h							
	[3:2]	PLL_IF_GC	0h							
3168h	[7:0]	INCKSEL3	68h							
316Ah	[2:0]	INCKSEL4	3h							
3199h	[4]	HADD	0h	0h						
	[5]	VADD								
319Dh	[0]	MDBIT	1h	0h / 1h						0: 10 bit, 1: 12 bitt
319Eh	[0]	SYS_MODE	0h	Set according to INCK Refer to page 73						
3300h	[1:0]	TCYCLE	0h	0h						
341Ch	[7:0]	ADBIT1	047h	10bit AD : 1FFh 12bit AD : 047h						
341Dh	[1:0]									
3A01h	[2:0]	LANEMODE	3h	1h	3h					
3A18h	[7:0]	TCLK POST	008Fh	008Fh	007Fh	008Fh	008Fh	007Fh	008Fh	Global timing
3A19h	[7:0]									
3A1Ah	[7:0]	TCLK PREPARE	004Fh	004Fh	0037h	004Fh	004Fh	0037h	004Fh	
3A1Bh	[7:0]									
3A1Ch	[7:0]	TCLK TRAIL	004Fh	0047h	0037h	0047h	0047h	0037h	0047h	
3A1Dh	[7:0]									
3A1Eh	[7:0]	TCLK ZERO	0137h	0137h	00F7h	0137h	0137h	00F7h	0137h	
3A1Fh	[7:0]									

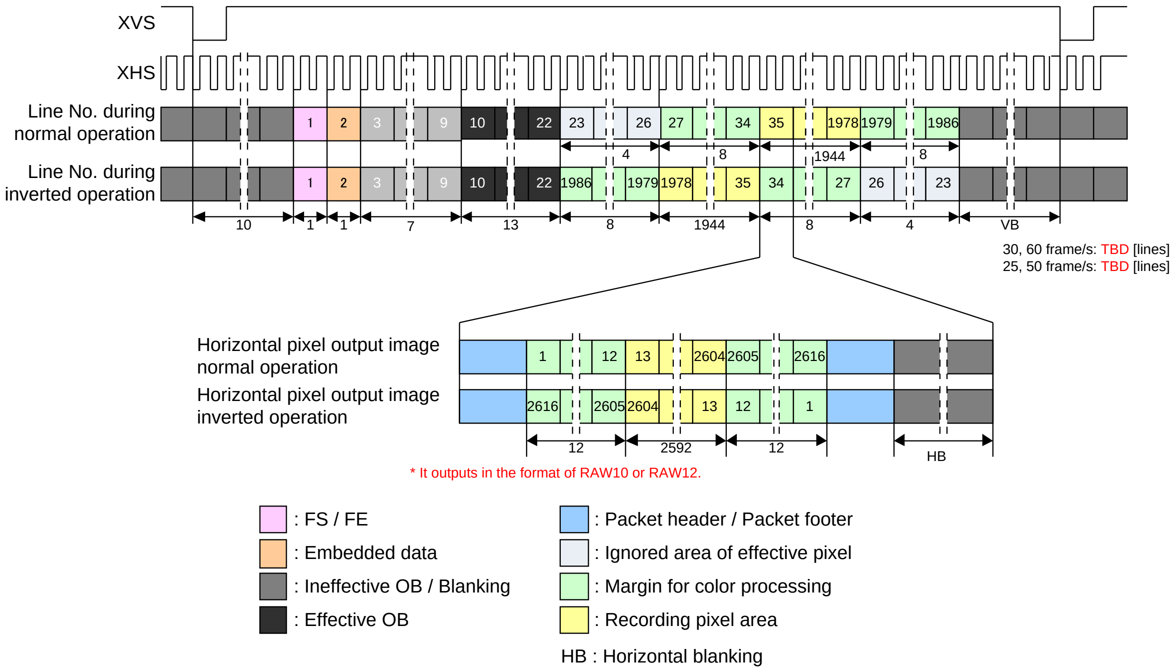
Address	bit	Register Name	Initial Value	CSI-2 serial						Remarks
				2 lane	4 lane					
				30 / 25 [frame /s]	30 / 25 [frame /s]	30 / 25 [frame /s]	60 /50 [frame /s]	30 /25 [frame /s]	30 / 25 [frame /s]	
AD Conversion				10	10	10	10	12	12	
Output bit width				10	10	10	10	12	12	
Data rate				1188	891	1188	1188	891	1188	
3A20h	[7:0]	THS PREPARE	004Fh	004Fh	003Fh	004Fh	004Fh	003Fh	004Fh	
3A21h	[7:0]									
3A22h	[7:0]	THS ZERO	0087h	0087h	006Fh	0087h	0087h	006Fh	0087h	
3A23h	[7:0]									
3A24h	[7:0]	THS TRAIL	004Fh	004Fh	003Fh	004Fh	004Fh	003Fh	004Fh	
3A25h	[7:0]									
3A26h	[7:0]	THS EXIT	007Fh	007Fh	005Fh	007Fh	007Fh	005Fh	007Fh	
3A27h	[7:0]									
3A28h	[7:0]	TLPX	003Fh	003Fh	002Fh	003Fh	003Fh	002Fh	003Fh	
3A29h	[7:0]									

Set the following register depending on a read out mode.

Address	bit	Initial Value	Vertical readout direction	
			Normal	Inverted
3078h	[7:0]	01h	01h	01h
3079h	[7:0]	02h	02h	02h
307Ah	[7:0]	FFh	FFh	FFh
307Bh	[7:0]	02h	02h	02h
307Ch	[7:0]	00h	00h	00h
307Dh	[7:0]	00h	00h	00h
307Eh	[7:0]	00h	00h	00h
307Fh	[7:0]	00h	00h	00h
3080h	[7:0]	01h	01h	01h
3081h	[7:0]	02h	02h	FEh
3082h	[7:0]	FFh	FFh	FFh
3083h	[7:0]	02h	02h	FEh
3084h	[7:0]	00h	00h	00h
3085h	[7:0]	00h	00h	00h
3086h	[7:0]	00h	00h	00h
3087h	[7:0]	00h	00h	00h
30A4h	[7:0]	33h	33h	33h
30A8h	[7:0]	10h	10h	10h
30A9h	[7:0]	04h	04h	04h
30ACh	[7:0]	00h	00h	00h
30ADh	[7:0]	00h	00h	00h
30B0h	[7:0]	10h	10h	10h
30B1h	[7:0]	08h	08h	08h
30B4h	[7:0]	00h	00h	00h
30B5h	[7:0]	00h	00h	00h
30B6h	[7:0]	0000h	0000h	01FAh
30B7h	[0]			
3112h	[7:0]	0008h	0008h	0008h
3113h	[0]			
3116h	[7:0]	0008h	0008h	0002h
3117h	[0]			



Pixel Array Image Drawing in All scan mode



Drive Timing Chart for All scan mode

Horizontal/Vertical 2/2-line binning scan mode

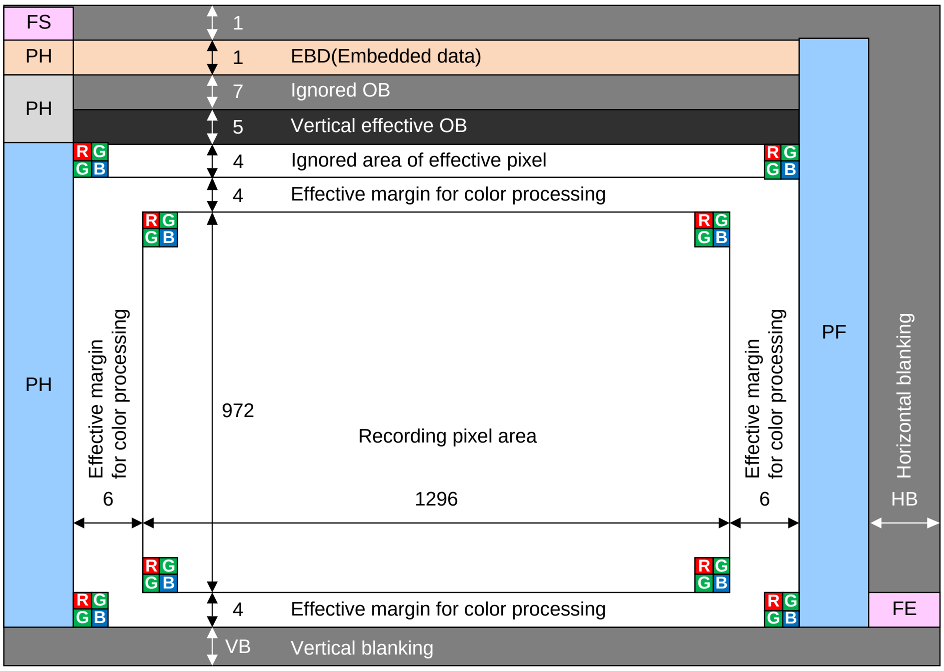
List of Setting Register

<table>
<tr><th rowspan="3">Address</th><th rowspan="3">bit</th><th rowspan="3">Register Name</th><th rowspan="3">Initial Value</th><th colspan="7">CSI-2 serial</th><th rowspan="2">Remarks</th></tr>
<tr><th colspan="3">2 lane</th><th colspan="4">4 lane</th></tr>
<tr><th>30 / 25 [frame/s]</th><th>30 / 25 [frame/s]</th><th>60 / 50 [frame/s]</th><th>30 /25 [frame/s]</th><th>60 /50 [frame/s]</th><th>30 / 25 [frame/s]</th><th>60 /50 [frame/s]</th><th></th></tr>
<tr><td colspan="4">AD Conversion</td><td>10</td><td>10</td><td>10</td><td>10</td><td>10</td><td>10</td><td>10</td><td></td></tr>
<tr><td colspan="4">Output bit width</td><td>12</td><td>12</td><td>12</td><td>12</td><td>12</td><td>12</td><td>12</td><td></td></tr>
<tr><td colspan="4">Data rate</td><td>891</td><td>1188</td><td>1188</td><td>891</td><td>891</td><td>1188</td><td>1188</td><td></td></tr>
<tr><td>3018h</td><td>[3:0]</td><td>WINMODE</td><td>0h</td><td colspan="7">1h</td><td></td></tr>
<tr><td>3030h</td><td>[7:0]</td><td rowspan="3">VMAX</td><td rowspan="3">1194h</td><td colspan="7" rowspan="3">1194h</td><td rowspan="3">25 /30 / 50 / 60 [frame/s]</td></tr>
<tr><td>3031h</td><td>[7:0]</td></tr>
<tr><td>3032h</td><td>[3:0]</td></tr>
<tr><td>3034h</td><td>[7:0]</td><td rowspan="2">HMAX</td><td rowspan="2">0226h</td><td rowspan="2">0226h / 0280h</td><td rowspan="2">0226h / 0280h</td><td rowspan="2">0113h / 0140h</td><td rowspan="2">0226h / 0280h</td><td rowspan="2">0113h / 0140h</td><td rowspan="2">0226h / 0280h</td><td rowspan="2">0113h / 0140h</td><td rowspan="2">30/ 60[frame/ s]
25/ 50[frame/ s]</td></tr>
<tr><td>3035h</td><td>[7:0]</td></tr>
<tr><td>304Ch</td><td>[5:0]</td><td>OPB_SIZE_V</td><td>14h</td><td colspan="7">14h</td><td></td></tr>
<tr><td>304Eh</td><td>[7:0]</td><td>HREVERSE</td><td>00h</td><td colspan="7">00h / 01h</td><td>0: Normal,
1: Inverted</td></tr>
<tr><td>304Fh</td><td>[7:0]</td><td>VREVERSE</td><td>00h</td><td colspan="7">00h / 01h</td><td>0: Normal
1: Inverted</td></tr>
<tr><td>3050h</td><td>[7:0]</td><td>ADBIT</td><td>01h</td><td colspan="7">00h</td><td></td></tr>
<tr><td>3056h</td><td>[7:0]</td><td rowspan="2">Y_OUT_SIZE</td><td rowspan="2">74Ch</td><td colspan="7" rowspan="2">3D8h</td><td rowspan="2"></td></tr>
<tr><td>3057h</td><td>[7:0]</td></tr>
<tr><td>3072h</td><td>[7:0]</td><td rowspan="2">AREA2_WIDTH_1</td><td rowspan="2">0028h</td><td colspan="7" rowspan="2">0030h</td><td rowspan="2"></td></tr>
<tr><td>3073h</td><td>[4:0]</td></tr>
<tr><td>3074h</td><td>[7:0]</td><td rowspan="2">AREA3_ST_ ADR_1</td><td rowspan="2">00B0h</td><td colspan="7" rowspan="2">Vertical read out
Normal : 00A8h , Inverted : 1018h</td><td rowspan="2"></td></tr>
<tr><td>3075h</td><td>[4:0]</td></tr>
<tr><td>3076h</td><td>[7:0]</td><td rowspan="2">AREA3_WIDTH_1</td><td rowspan="2">0F58h</td><td colspan="7" rowspan="2">0F60h</td><td rowspan="2"></td></tr>
<tr><td>3077h</td><td>[4:0]</td></tr>
<tr><td>314Ch</td><td>[7:0]</td><td rowspan="2">INCKSEL1</td><td rowspan="2">080h</td><td colspan="7" rowspan="6">Set according to INCK
Refer to page 73</td><td rowspan="6"></td></tr>
<tr><td>314Dh</td><td>[7:0]</td></tr>
<tr><td rowspan="2">315Ah</td><td>[1:0]</td><td>INCKSEL2</td><td>3h</td></tr>
<tr><td>[3:2]</td><td>PLL_IF_GC</td><td>0h</td></tr>
<tr><td>3168h</td><td>[7:0]</td><td>INCKSEL3</td><td>68h</td></tr>
<tr><td>316Ah</td><td>[7:0]</td><td>INCKSEL4</td><td>7Fh</td></tr>
<tr><td rowspan="2">3199h</td><td>[4]</td><td>HADD</td><td rowspan="2">0h</td><td colspan="7" rowspan="2">3h</td><td rowspan="2"></td></tr>
<tr><td>[5]</td><td>VADD</td></tr>
<tr><td>319Dh</td><td>[7:0]</td><td>MDBIT</td><td>01h</td><td colspan="7">0h / 1h</td><td>0: 10 bit
1: 12 bit</td></tr>
<tr><td>319Eh</td><td>[7:0]</td><td>SYS_MODE</td><td>01h</td><td colspan="7">Set according to INCK
Refer to page 73</td><td></td></tr>
<tr><td>319Eh</td><td>[7:0]</td><td>TCYCLE</td><td>00h</td><td colspan="7">01h</td><td></td></tr>
<tr><td>341Ch</td><td>[7:0]</td><td rowspan="2">ADBIT1</td><td rowspan="2">047h</td><td colspan="7" rowspan="2">1FFh</td><td rowspan="2"></td></tr>
<tr><td>341Dh</td><td>[7:0]</td></tr>
<tr><td>3A01h</td><td>[7:0]</td><td>LANE MODE</td><td>03h</td><td colspan="3">01h</td><td colspan="4">03h</td><td></td></tr>
<tr><td>3A18h</td><td>[7:0]</td><td rowspan="2">TCLK POST</td><td rowspan="2">008Fh</td><td rowspan="2">007Fh</td><td rowspan="2">008Fh</td><td rowspan="2">008Fh</td><td rowspan="2">007Fh</td><td rowspan="2">007Fh</td><td rowspan="2">008Fh</td><td rowspan="2">008Fh</td><td rowspan="8">Global timing</td></tr>
<tr><td>3A19h</td><td>[7:0]</td></tr>
<tr><td>3A1Ah</td><td>[7:0]</td><td rowspan="2">TCLK PREPARE</td><td rowspan="2">004Fh</td><td rowspan="2">0037h</td><td rowspan="2">004Fh</td><td rowspan="2">004Fh</td><td rowspan="2">0037h</td><td rowspan="2">0037h</td><td rowspan="2">004Fh</td><td rowspan="2">004Fh</td></tr>
<tr><td>3A1Bh</td><td>[7:0]</td></tr>
<tr><td>3A1Ch</td><td>[7:0]</td><td rowspan="2">TCLK TRAIL</td><td rowspan="2">004Fh</td><td rowspan="2">0037h</td><td rowspan="2">0047h</td><td rowspan="2">0047h</td><td rowspan="2">0037h</td><td rowspan="2">0037h</td><td rowspan="2">0047h</td><td rowspan="2">0047h</td></tr>
<tr><td>3A1Dh</td><td>[7:0]</td></tr>
<tr><td>3A1Eh</td><td>[7:0]</td><td rowspan="2">TCLK ZERO</td><td rowspan="2">0137h</td><td rowspan="2">00F7h</td><td rowspan="2">0137h</td><td rowspan="2">0137h</td><td rowspan="2">00F7h</td><td rowspan="2">00F7h</td><td rowspan="2">0137h</td><td rowspan="2">0137h</td></tr>
<tr><td>3A1Fh</td><td>[7:0]</td></tr>
</table>

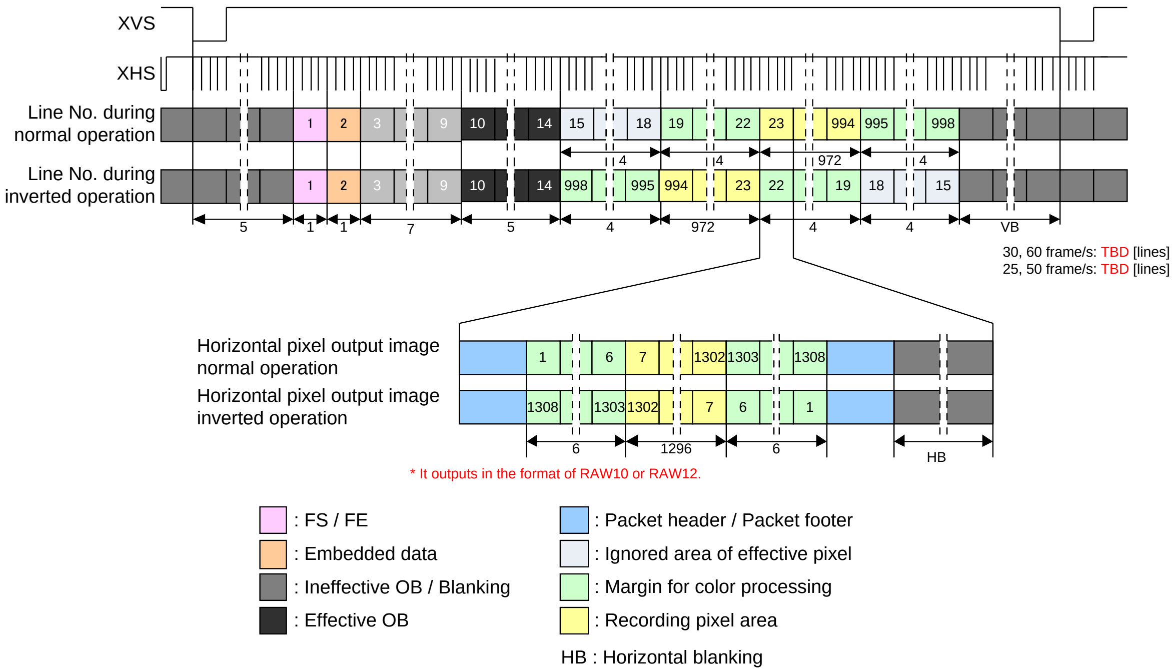
Address	bit	Register Name	Initial Value	CSI-2 serial							Remarks
				2 lane			4 lane				
				30 / 25 [frame/s]	30 / 25 [frame/s]	60 / 50 [frame/s]	30 /25 [frame/s]	60 /50 [frame/s]	30 / 25 [frame/s]	60 /50 [frame/s]	
AD Conversion				10	10	10	10	10	10	10	
Output bit width				12	12	12	12	12	12	12	
Data rate				891	1188	1188	891	891	1188	1188	
3A20h	[7:0]	THS PREPARE	004Fh	003Fh	004Fh	004Fh	003Fh	003Fh	004Fh	004Fh	
3A21h	[7:0]										
3A22h	[7:0]	THS ZERO	0087h	006Fh	0087h	0087h	006Fh	006Fh	0087h	0087h	
3A23h	[7:0]										
3A24h	[7:0]	THS TRAIL	004Fh	003Fh	004Fh	004Fh	003Fh	003Fh	004Fh	004Fh	
3A25h	[7:0]										
3A26h	[7:0]	THS EXIT	007Fh	005Fh	007Fh	007Fh	005Fh	005Fh	007Fh	007Fh	
3A27h	[7:0]										
3A28h	[7:0]	TLPX	003Fh	002Fh	003Fh	003Fh	002Fh	002Fh	003Fh	003Fh	
3A29h	[7:0]										

Set the following register depending on a read out mode.

Address	bit	Initial Value	Vertical readout direction	
			Normal	Inverted
3078h	[7:0]	01h	04h	04h
3079h	[7:0]	02h	FDh	FDh
307Ah	[7:0]	FFh	04h	04h
307Bh	[7:0]	02h	FEh	FEh
307Ch	[7:0]	00h	04h	04h
307Dh	[7:0]	00h	FBh	FBh
307Eh	[7:0]	00h	04h	04h
307Fh	[7:0]	00h	02h	02h
3080h	[7:0]	01h	04h	FCh
3081h	[7:0]	02h	FDh	05h
3082h	[7:0]	FFh	04h	FCh
3083h	[7:0]	02h	FEh	02h
3084h	[7:0]	00h	04h	FCh
3085h	[7:0]	00h	FBh	03h
3086h	[7:0]	00h	04h	FCh
3087h	[7:0]	00h	02h	FEh
30A4h	[7:0]	33h	77h	77h
30A8h	[7:0]	10h	20h	20h
30A9h	[7:0]	04h	00h	00h
30ACh	[7:0]	00h	08h	08h
30ADh	[7:0]	00h	08h	78h
30B0h	[7:0]	10h	20h	20h
30B1h	[7:0]	08h	00h	00h
30B4h	[7:0]	00h	10h	10h
30B5h	[7:0]	00h	10h	70h
30B6h	[7:0]	0000h	0000h	01F2h
30B7h	[0]			
3112h	[7:0]	0008h	0010h	0010h
3113h	[0]			
3116h	[7:0]	0008h	0010h	0002h
3117h	[0]			



Pixel Array Image Drawing in Horizontal /Vertical 2/2-line binnign scan mode



Drive Timing Chart for Horizontal /Vertical 2/2-line binnign scan mode

Window Cropping Mode

Sensor signals are cut out and read out in arbitrary positions.
Cropping position is set, regarding effective pixel start position as origin (48, 176) in all pixel scan mode. Cropping is available from all-pixel scan mode and vertical, horizontal period and frame rate are fixed to the value for this mode. Pixels cropped by horizontal cropping setting are output with left justified and that extends the horizontal blanking period.
Window cropping image is shown in the figure below.
This fanction support only All-pixel scan mode.

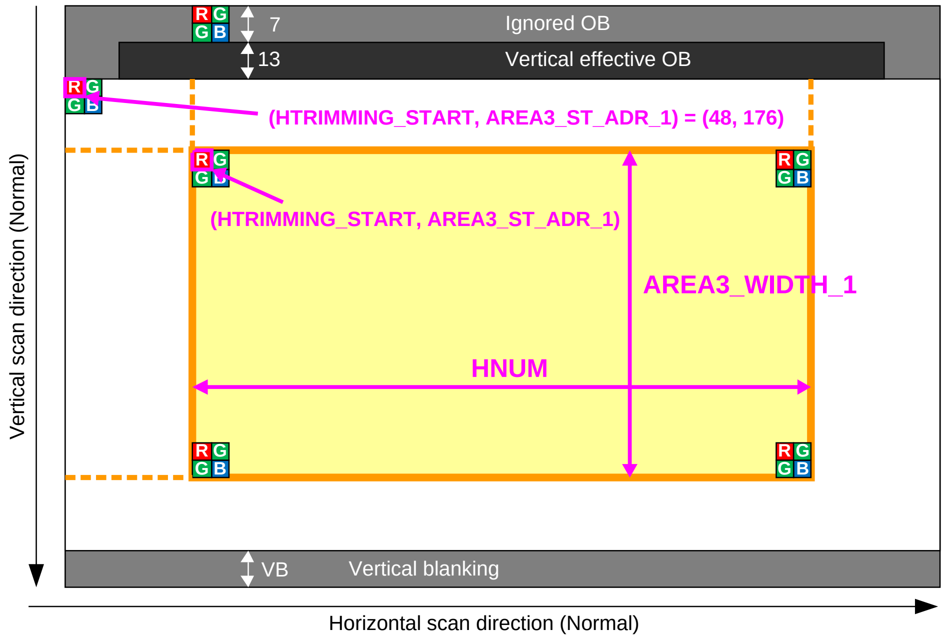


Image Drawing of Window Cropping Mode

Restrictions on Window cropping mode
The register settings should satisfy following conditions:

Set WINMODE: 4h.

48 ≦ HTRIMMING_START + HNUM ≦ 2664
HTRIMMING_START = 48 + N×12
312 ≦HNUM
Set HNUM to a multiple of 24.
(N is integer equal or more than 0)

AREA3_ST_ADR_1 = 176 + M×4
372 × 2 ≦ AREA3_WIDTH_1 ≦ 1964 × 2
Set AREA3_WIDTH_1 to twice the number of the lines
(M is integer equal or more than 0)

Set AREA3_WIDTH_1 to multiple of 4.

UNREAD_ED_ADR = AREA3_ST_ADR_1 + AREA3_WIDTH_1 + 208
In case of UNREAD_ED_ADR ＞ 4172 , set UNREAD_ED_ADR = 4172

V_{TTL} (1frame line length or VMAX) ≧ AREA3_WIDTH_1 + 96

In case of 176 ≦ AREA3_ST_ADR_1 ＜276 ,set
UNRD_LINE_MAX = 0
BLACK_OFSET_ADR = 0

In case of 276 ≦ AREA3_ST_ADR_1 , set
UNRD_LINE_MAX = 100
BLACK_OFSET_ADR = 18

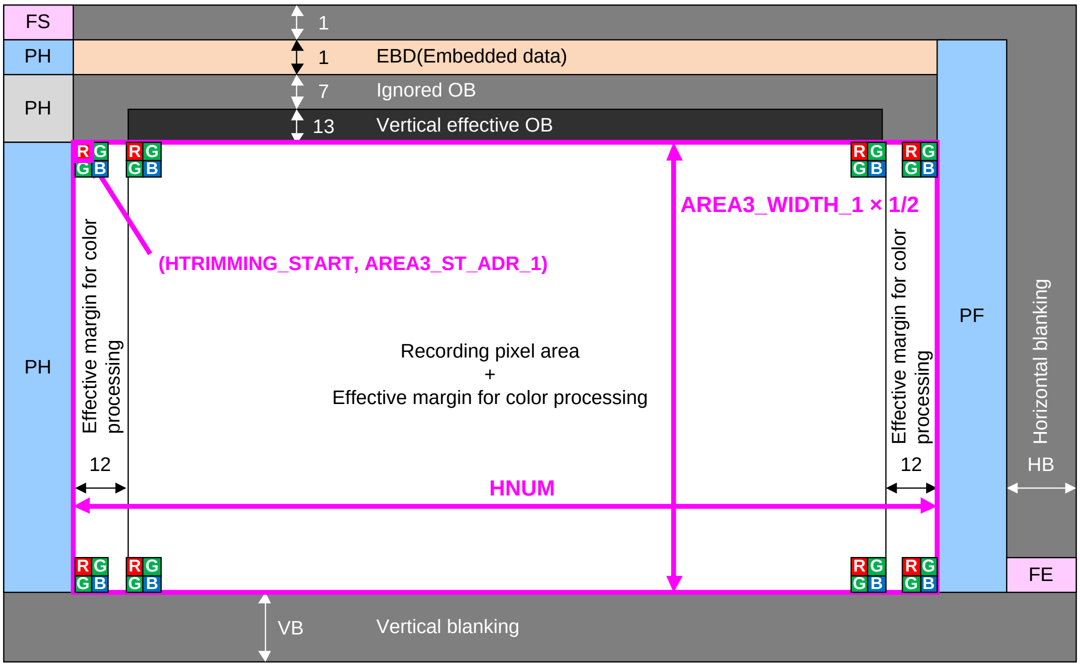
Frame rate on Window cropping mode
Frame rate [frame/s] = 1 / (V_{TTL} × (1H period))

1H period (unit: [μs]) : Fix 1H time in a mode before cropping and calculate it by the value of "Number of INCK in 1H" in the table of "Operating Mode" and "List of Operation Modes and Output Rates".

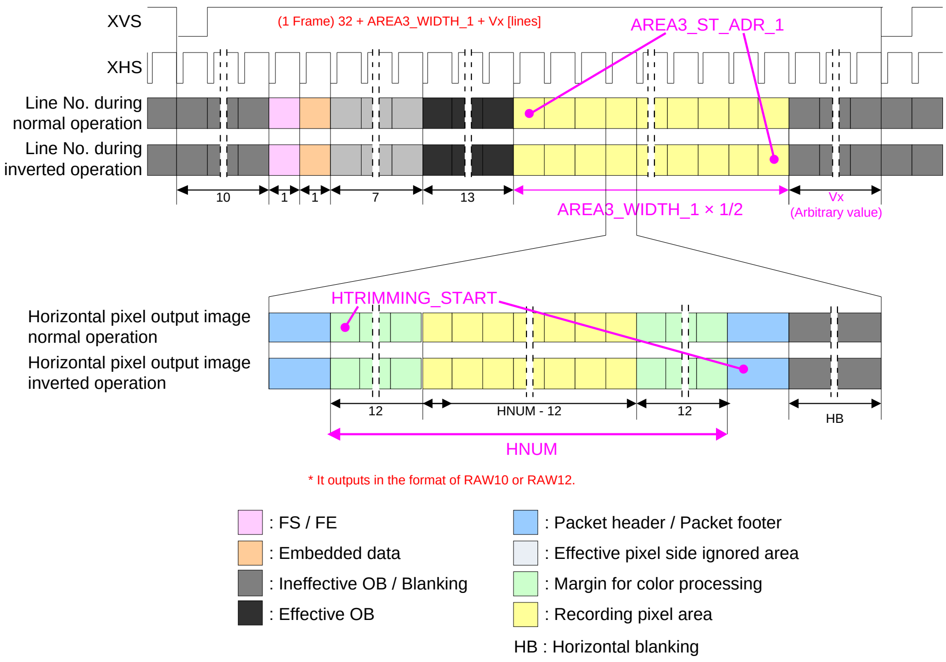
The example of window cropping setting is shown below.
The frame rate is maximum setting as each image format. For adjust the frame rate, please extend the VMAX or the number of lines per frame.

Example of Window cropping Mode Setting

Recording Pixels				1920×1080		Remarks
AD Conversion [bit]				10	12	
Output bit width [bit]				10	12	
Data rate [Mbps/lane]				1188	1188	
Frame rate [frame/s]				118	118	
Address	bit	Register Name	Initial Value			
3018h	[3:0]	WINMODE	0h	4h	4h	
3030h	[7:0]	VMAX	1194h	08F0h	08F0h	
3031h	[7:0]					
3032h	[3:0]					
3034h	[7:0]	HMAX	0226h	0226h	0226h	
3035h	[7:0]					
302Ch	[7:0]	HTRIMMING_START	0030h	0180h	0180h	
302Dh	[7:0]					
302Eh	[7:0]	HNUM	0A38h	0798h	0798h	
302Fh	[3:0]					
3074h	[7:0]	AREA3_ST_ADR_1	00B0h	0260h	0260h	
3075h	[4:0]					
3076h	[7:0]	AREA3_WIDTH_1	0F58h	0890h	0890h	
3077h	[4:0]					
30C6h	[7:0]	BLACK_OFSET_ADR	0000h	0012h	0012h	
30C7h	[4:0]					
30CEh	[7:0]	UNRD_LINE_MAX	0000h	0064h	0064h	
30CFh	[4:0]					
30D8h	[7:0]	UNREAD_ED_ADR	104Ch	0BC0h	0BC0h	
30D9h	[4:0]					



Pixel Array Image Drawing in Window Cropping mode (CSI-2 serial output)



Drive Timing Chart for Window Cropping mode (CSI-2 serial output)

Description of Various Function

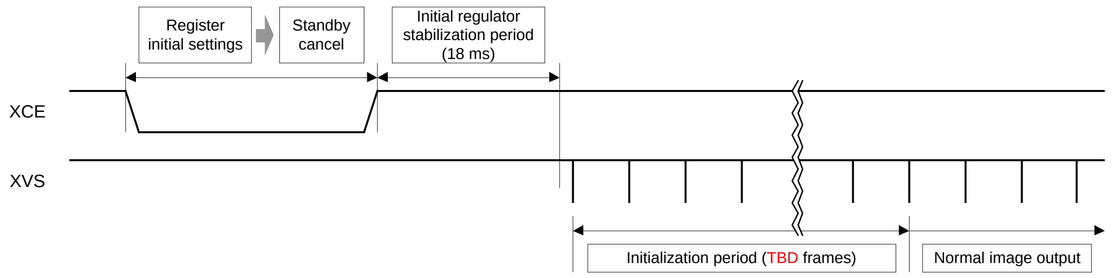
Standby Mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing "1" to the standby control register STANDBY. Standby mode is also established after power-on or other system reset operation.

List of Standby Mode Setting

Register name	Register details			Initial value	Setting value	Status	Remarks
	Register	Address	bit				
STANDBY	—	3000h	[0]	1	1	Standby	Register communication is executed in standby mode.
					0	Operating	

The serial communication registers hold the previous values. However, the address registers transmitted in standby mode are overwritten. The serial communication block operates even in standby mode, so standby mode can be canceled by setting the STANDBY register to "0". Some time is required for sensor internal circuit stabilization after standby mode is canceled. After standby mode is canceled, a normal image is output from the TBD frames after internal regulator stabilization (18 ms or more).



Sequence from Standby Cancel to Stable Image Output

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode. The switching is made by the XMASTER pin. Establish the XMASTER pin status before canceling the system reset. (Do not switch this pin status during operation.)

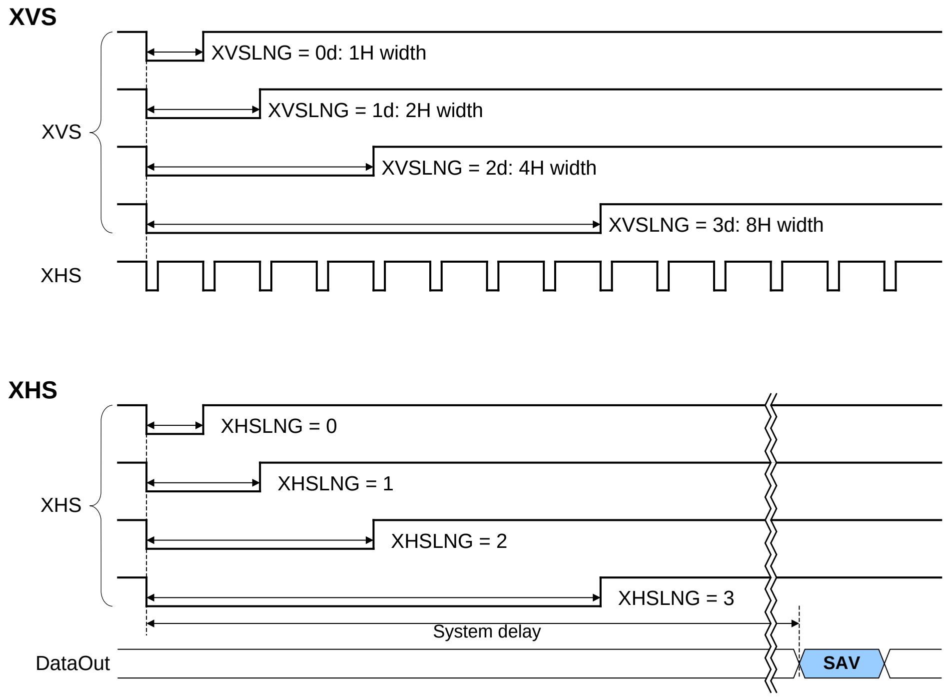
Input a vertical sync signal to XVS and input a horizontal sync signal to XHS when a sensor is in slave mode.
For sync signal interval, input data lines to output for vertical sync signal and 1H period designated in each operating mode for horizontal sync signal. See the section of "Operating mode" for the number of output data line and 1H period.
Set the XMSTA register to “0” in order to start the operation after setting to master mode. In addition, set the count number of sync signal in vertical direction by the VMAX [19:0] register and the clock number in horizontal direction by the HMAX [15:0] register. See the description of Operation Mode for details of the section of “Operating Modes”.

List of Slave and Master Mode Setting

Pin name	Pin processing	Operating mode	Remarks
XMASTER pin	Fixed to Low	Master mode	High: OV_{DD} Low: GND
	Fixed to High	Slave mode	

List of Register in Master Mode

Register name	Register details			Initial value	Setting value	Remarks
	Register	Address	bit			
XMSTA	—	3002h	[0]	1h	1: Master operation ready 0: Master operation start	The master operation starts by setting 0.
VMAX [19:0]	VMAX [7:0]	3030h	[7:0]	01194h	See the item of each drive mode.	Line number per frame designated
	VMAX [15:8]	3031h	[7:0]			
	VMAX [19:16]	3032h	[4:0]			
HMAX [15:0]	HMAX [7:0]	3034h	[7:0]	0226h	See the item of each drive mode.	Clock number per line designated
	HMAX [15:8]	3035h	[7:0]			
XVSLNG [5:4]	—	31D4h	[5:4]	0h	0: 1H, 1: 2H, 2: 4H, 3: 8H	XVS low level pulse width designated
XHSLNG [5:4]	—	31D5h	[4]	0h	0: 16clock, 1: 32clock 2: 64clock, 3: 128clock See the next	XHS low level pulse width designated
XVSOUTSEL [1:0]	—	31A0h	[1:0]	2h	0: Fixed to Low 2: VSYNC output Others: Setting prohibited	
XHSOUTSEL [1:0]	—		[3:2]	2h	0: Fixed to Low 2: HSYNC output Others: Setting prohibited	



XVS/XHS output waveform in sensor master mode

The XVS and XHS are output in timing that set 0 to the register XMSTA. If set 0 to XMSTA during standby, the XVS and XHS are output just after standby is released. The XVS and XHS are output asynchronous with other input or output signals. In addition, the output signals are output with a undefined latency time (system delay) relative to the XHS. Therefore, refer to the sync codes output from the sensor and perform synchronization.

Gain Adjustment Function

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block. The total of analog gain and digital gain can be set up to TBDdB by the GAIN [7:0] register setting. The same setting is applied in all colors.

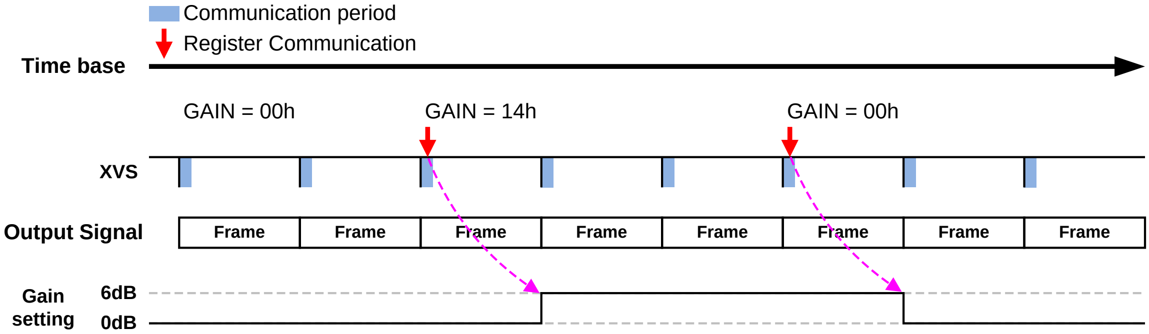
The value which is 10/3 times the gain is set to register. (0.3 dB step)

Example)
When set to 6 dB: 6 × 10/3 = 20d; GAIN [7:0] = 14h
When set to 12.6 dB: 12.6 × 10/3 = 42d; GAIN [7:0] = 2Ah

List of PGC Register

Register name	Register details (Chip ID = 81h)				Initial value	Setting value	Remarks
	Register	MSB Address	Address ( ) : I^2C	bit		Setting range	
GAIN [10:0]	GAIN [7:0]	00h	E8h (30E8h)	[7:0]	00h	00h-TBDh (0d-TBDd)	Setting value: Gain [dB] × 10/3 (0.3 dB step)
	GAIN [10:8]		E9h (30E9h)	[3:0]	00h		

The gain setting is reflected at the next frame that the communication is performed as shown below.



Gain Reflection Timing

Black Level Adjustment Function

The black level offset (offset variable range: 000h to 3FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL [9:0] register.
Note that the offset unit changes according to the output bit setting.
When the output data length is 10-bit output, increasing the register setting value by 1h increases the black level by 1 LSB. When the output data length is 12-bit output, increasing the register setting value by 1h increases the black level by 4 LSB.

Use with values shown below is recommended.
10-bit output: 032h (50d)
12-bit output: 032h (200d)

List of Black Level Adjustment Register

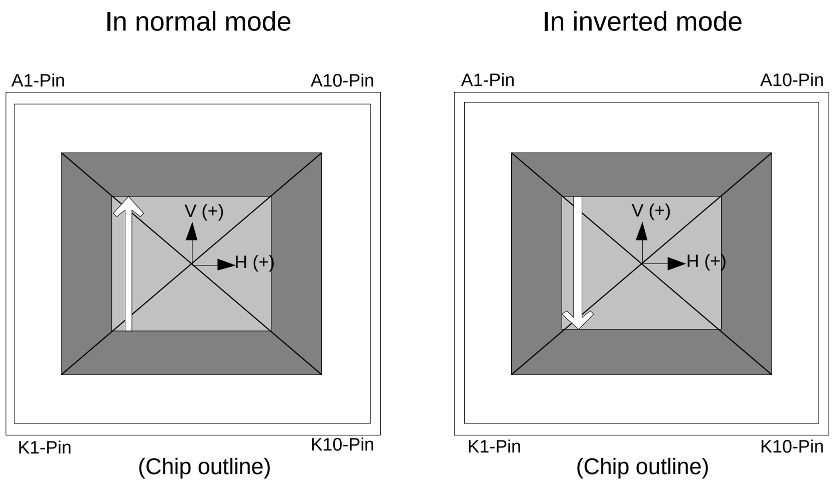
Register name	Register details			Initial value	Setting value
	Register	Address	bit		
BLKLEVEL [9:0]	BLKLEVEL [7:0]	3302h	[7:0]	032h	000h to 3FFh
	BLKLEVEL [9:8]	3303h	[1:0]		

Normal Operation and Inverted Operation

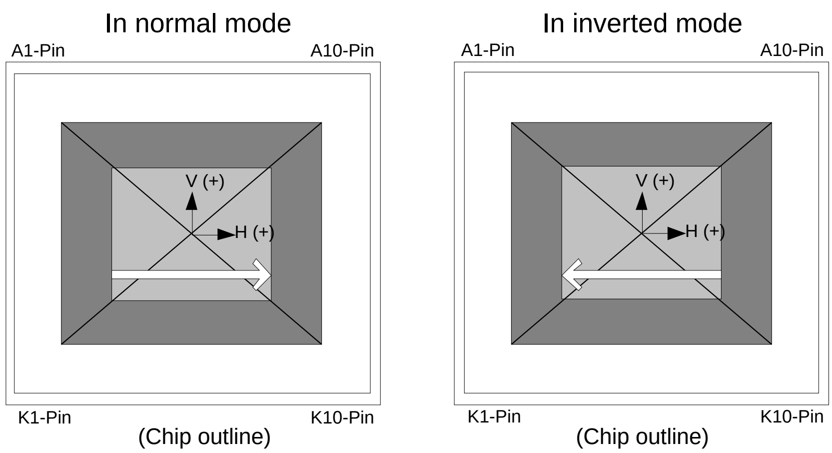
The sensor readout direction (normal / inverted) in vertical direction can be switched by VREVERSE register settings and in horizontal direction can be switched by the HREVERSE register setting. See the section of “Operating Modes” for the order of readout lines in normal and inverted modes. See the section of “List of Setting Register” for the other register settings. One invalid frame is generated when reading immediately after the readout direction change in order to switch the normal operation and inversion between frames.

List of Drive Direction Setting Register

Address	bit	Register name	Initial value	Normal	Inverted
304Eh	[0]	HREVERSE	00h	00h	01h
304Fh	[0]	VREVERSE	00h	00h	01h



Normal and Inverted Drive Outline in Vertical Direction (TOP VIEW)



Normal and Inverted Drive Outline in Horizontal Direction (TOP VIEW)

Shutter and Integration Time Settings

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

Example of Integration Time Setting

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period - SHR0 × (1H period)

*1 The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is designated in 1H units, so the time is determined by (Number of lines × 1H period).

*2 See “Operating Modes” for the 1H period.

In this section, the shutter operation and storage time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

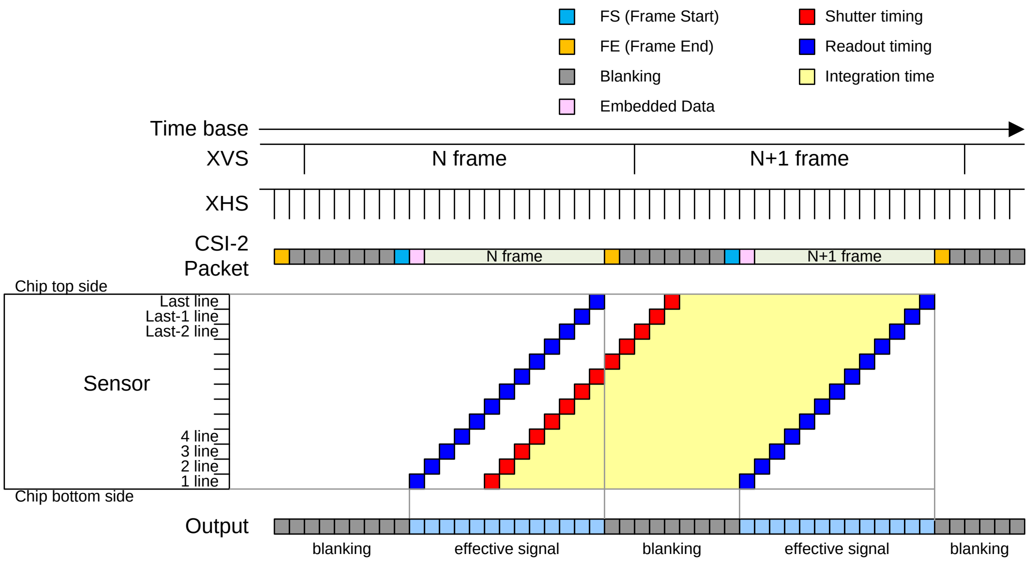


Image Drawing of Shutter Operation

Normal Exposure Operation (Controlling the Integration Time in 1H Units)

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHR0 [19:0] register. Set SHR0 [19:0] to a value between 9 and (Number of lines per frame - 1) in All-pixel scan mode. Set SHR0 [19:0] to a value between 17 and (Number of lines per frame - 1) in Horizontal/Vertical 2/2-line binning scan mode. When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit.
When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX register.
The number of lines per frame differs according to the operating mode.

Registers Used to Set the Integration Time in 1H Units

Register name	Register details			Initial value	Setting value
	Register	Address	bit		
SHR0 [19:0]	SHR0 [7:0]	3058h	[7:0]	00009h	Sets the shutter sweep time. All pixel scan : 9 to (Number of lines per frame - 1) Horizontal/Vertical 2/2-line binning scan : 17 to (Number of lines per frame - 1) * Others: Setting prohibited
	SHR0 [15:8]	3059h	[7:0]		
	SHR0 [19:16]	305Ah	[3:0]		
VMAX [19:0]	VMAX [7:0]	3030h	[7:0]	01194h	Sets the number of lines per frame (only in master mode). See “Operating Modes” for the setting value in each mode.
	VMAX [15:8]	3031h	[7:0]		
	VMAX [19:16]	3032h	[3:0]		

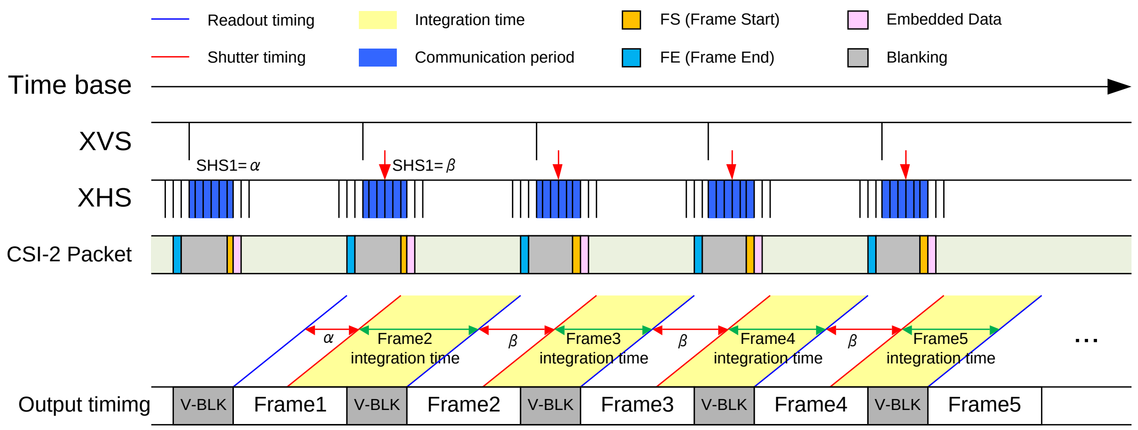


Image Drawing of Integration Time Control within a Frame

Long Exposure Operation (Control by Expanding the Number of Lines per Frame)

Long exposure operation can be performed by lengthening the frame period.
When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval.
When the sensor is operating in master mode, it is done by designating a larger register VMAX [19:0] value compared to normal operation. When the integration time is extended by increasing the number of lines, the rear V blanking increases by an equivalent amount.

Although the maximum value of long exposure operation changes in each modes, the maximum of long time exposure is approximately 1 s.
When set to a number of V lines or more than that noted for each operating mode, the imaging characteristics are not guaranteed during long exposure operation.

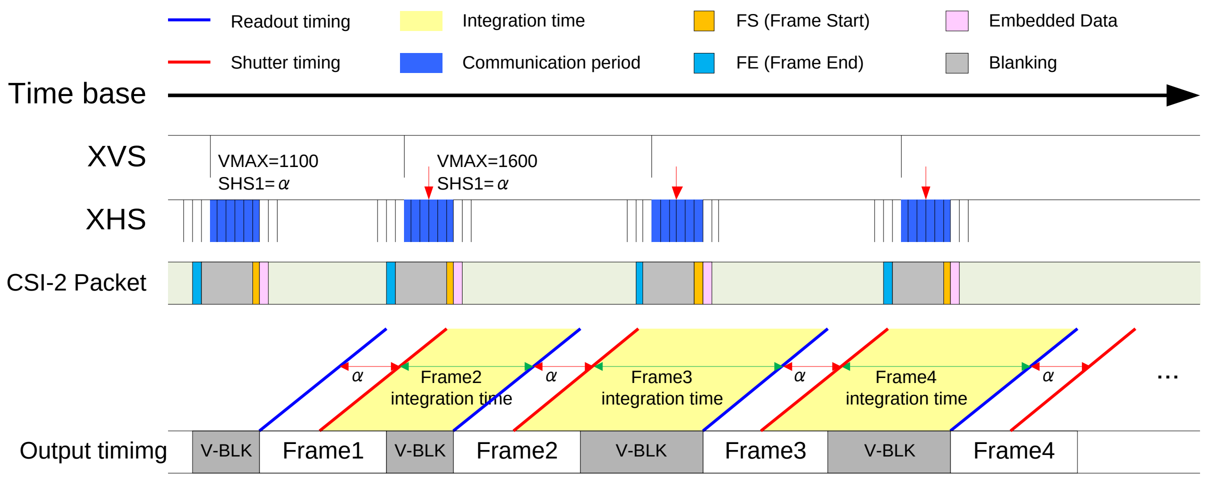


Image Drawing of Long Integration Time Control by Adjusting the Frame Period

Example of Integration Time Settings

The example of register setting for controlling the storage time is shown below.

Example of Integration Time Settings

Operation	Sensor setting (register)		Integration time
	VMAX*	SHR0**	
All-scan mode	4500	4499	1H
		⋮	⋮
		N	(4500 - N) H
		⋮	⋮
		9	4491H
Horizontal/Vertical 2/2-line binning scan mode	4500	4499	1H
		⋮	⋮
		N	(4500 - N) H
		⋮	⋮
		17	4483H

* In sensor master mode. In slave mode, the interval is the same as XVS input.
** The SHR0 setting value (N) is set All-scan mode between “9” and “the VMAX value (M) – 1”, Horizontal/Vertical 2/2-line binning scan mode between “17” and “the VMAX value (M) – 1”.

Signal Output
CSI-2 output

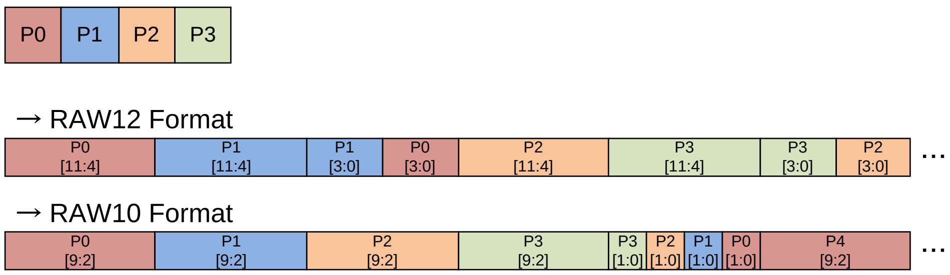
The output formats of this sensor support the following modes.

CSI-2 serial 2 Lane / 4 Lane, RAW10 / RAW12

The 2 Lane / 4 Lane serial signal output method using this sensor is described below.
Complied with the CSI-2, data is output using 2 Lane / 4 Lane. The image data is output from the CSI-2 output pin. The DMOP1/DMOM1 are called the Lane1 data signal, the DMOP2/DMOM2 are called the Lane2 data signal, the DMOP3/DMOM3 are called the Lane3 data signal, the DMOP4/DMOM4 are called the Lane4 data signal. In addition, the clock signals are output from DMCKP/DMCKM of the CSI-2 pins.
In 2 Lane mode, data is output from Lane1 and Lane2. In 4 Lane mode, data is output from Lane1, Lane2, Lane3 and Lane4. The bit rate maximum value is 1188 Mbps / Lane.
The select of RAW10 / RAW12 is set by the register: MDBIT [0] The number of output lanes is set by the register: LANEMODE [2:0]. Unused lanes (when setting 2 lanes; DMOP3 / DMOM3, DMOP4 / DMOM4) output signals conformed to MIPI standard.

Register name	Register details		Initial value	Setting value	Description
	Address	bit			
MDBIT	319Dh	[0]	1h	0h	RAW10
				1h	RAW12
LANEMODE [2:0]	3A01h	[2:0]	3h	1h	2Lane
				3h	4Lane
				-	Others:Setting prohibited

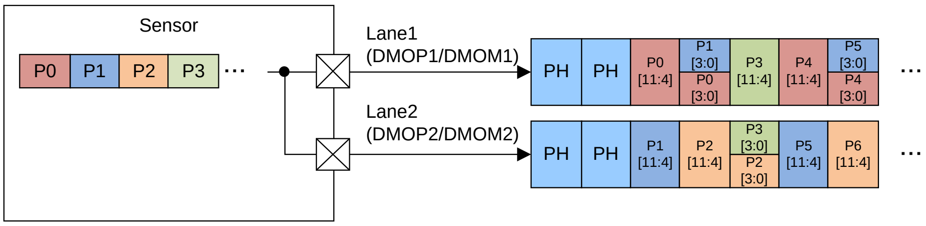
The formats of RAW12 and RAW10 are shown below.



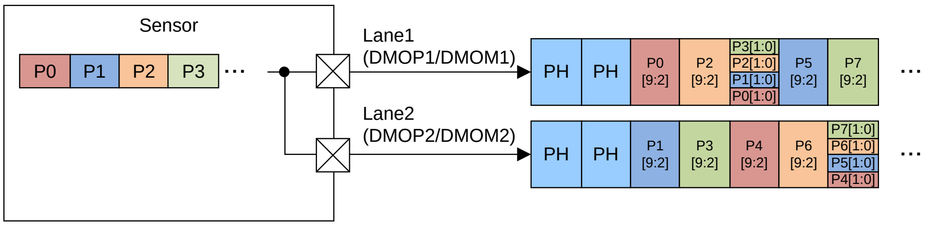
The Example of Format of RAW12 / RAW10

The each formal of 2 Lane and 4 Lane are shown below.

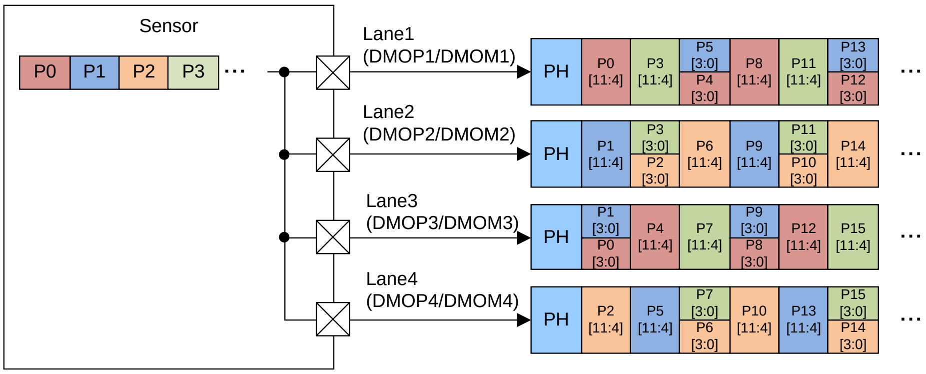
a) 2 Lane-RAW12



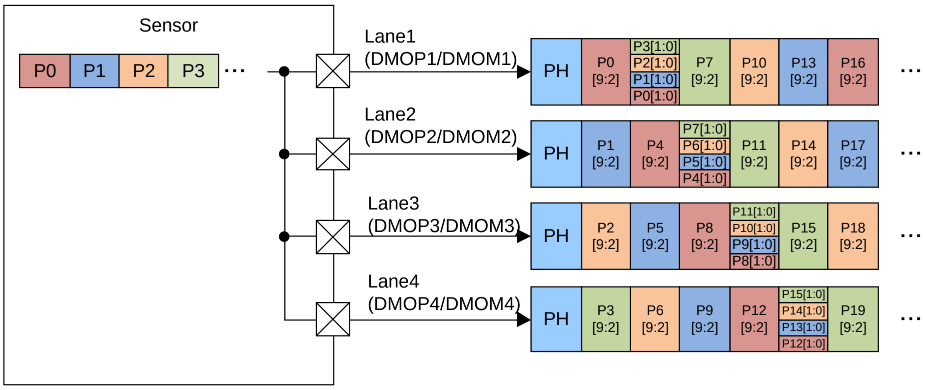
b) 2 Lane-RAW10



c) 4 Lane-RAW12



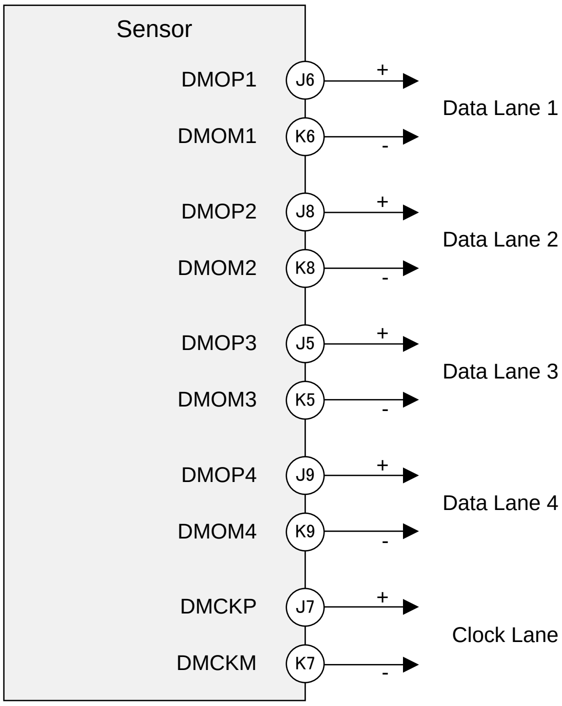
d)4 Lane-RAW10



2 Lane / 4 Lane Output Format

MIPI Transmitter

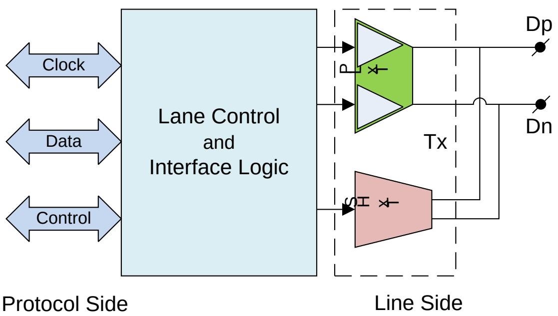
Output pins (DMOP1, DMOM1, DMOP2, DMOM2, DMOP3, DMOM3, DMOP4, DMOM4, DMCKP, DMCKM) are described in this section.



Relationship between Pin Name and MIPI Output Lane

The pixel signals are output by the CSI-2 High-speed serial interface.
See the MIPI Standard
・MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.10
・MIPI Alliance Specification for D-PHY Version 1.10

The CSI-2 transfers one bit with a pair of differential signals. The transmitter outputs differential current signal after converting pixel signals to it. Insert external resistance in differential pair in a series or use cells with a built-in resistance on the Receiver side. When inserting an external resistor, as close as possible to the Receiver. The differential signals maintain a constant interval and reach the receiver with the shortest wiring length possible to avoid malfunction. The maximum bit rate of each Lane are 1188 Mbps / Lane.



Universal Lane Module Functions

Number of Internal A/D Conversion Bits Setting

The number of internal A/D conversion bits can be selected from 10 bits or 12 bits by the register ADBIT. See the section of "Operating Modes" for the correspondence with each mode.

List of Bit Width Selection

Register name	Register details			Initial value	Setting value
	Register	Address	bit		
ADBIT	—	3050h	[0]	1h	0: 10 bit 1: 12 bit
ADBIT1[8:0]	ADBIT1[7:0]	341Ch	[7:0]	0047h	10 bit: 01FFh 12 bit: 0047h
	ADBIT1[8]	341Dh	[0]		

Output Signal Range

In CSI-2 output mode, the sensor output has either a 10 bit or 12 bit gradation, but output is not performed over the full range, and the maximum output value is the 3FFh value (10 bit output) and the FFFh one (12 bit output).
The output range for each output gradation is shown in the table below.

Output Gradation and Output Range (CSI-2 Output)

Output gradation	Output value	
	Min.	Max.
10 bit	000h	3FFh
12 bit	000h	FFFh

INCK Setting

The available operation mode varies according to INCK frequency. Input either 6-27 MHz ,37.125 MHz or 74.25 MHz for INCK frequency. The INCK setting register and the list of INCK setting are shown in the table below.

INCK Setting Register

Data late 1188Mbps / lane

Register name	Register details			Initial value	INCK					
	Register	Address	bit		6 [MHz]	12 [MHz]	18 [MHz]	24 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	—	300Ch	[7:0]	B6h	0Fh	1Eh	2Dh	3Bh	5Bh	B6h
CPWAIT_TIME	—	300Dh	[7:0]	7Fh	0Bh	15h	1Fh	2Ah	40h	7Fh
INCKSEL1	—	314D-4Ch	[8:0]	0080h	00C6h	00C6h	0084h	00C6h	0080h	0080h
INCKSEL2	—	315Ah	[1:0]	3h	0h	1h	1h	2h	2h	3h
PLL_IF_GC	—		[3:2]	0h	0h	0h	0h	0h	0h	0h
INCKSEL3	—	3168h	[7:0]	68h	A0h	A0h	6Bh	A0h	68h	68h
INCKSEL4	—	316Ah	[1:0]	7Fh	7Ch	7Dh	7Dh	7Eh	7Eh	7Fh
SYS_MODE	—	319Eh	[7:0]	00h	01h	01h	01h	01h	01h	01h

Data late 891Mbps / lane

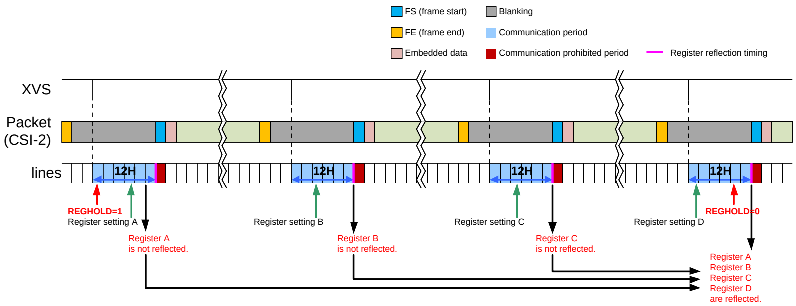
Register name	Register details			Initial value	INCK					
	Register	Address	bit		6 [MHz]	12 [MHz]	18 [MHz]	24 [MHz]	37.125 [MHz]	74.25 [MHz]
BCWAIT_TIME	—	300Ch	[7:0]	B6h	0Fh	1Eh	2Dh	3Bh	5Bh	B6h
CPWAIT_TIME	—	300Dh	[7:0]	7Fh	0Bh	15h	1Fh	2Ah	40h	7Fh
INCKSEL1	—	314D-4Ch	[8:0]	0080h	0129h	0129h	00C6h	0129h	00C0h	00C0h
INCKSEL2	—	315Ah	[1:0]	3h	0h	1h	1h	2h	2h	3h
PLL_IF_GC	—		[3:2]	0h	1h	1h	1h	1h	1h	1h
INCKSEL3	—	3168h	[7:0]	68h	A0h	A0h	6Bh	A0h	68h	68h
INCKSEL4	—	316Ah	[1:0]	7Fh	7Ch	7Dh	7Dh	7Eh	7Eh	7Fh
SYS_MODE	—	319Eh	[7:0]	00h	02h	02h	02h	02h	02h	02h

Register Hold Setting

Register setting can be transmitted with divided to several frames and it can be reflected globally at a certain frame by the register REGHOLD. Setting REGHOLD = 1 at the start of register communication period prevents the registers that are set thereafter from reflecting at the frame reflection timing. The registers that are set when setting REGHOLD = 1 are reflected globally by setting REGHOLD = 0 at the end of communication period of the desired frame to reflect the register.

Register Hold Setting Register

Register name	Register details			Initial value	Setting value
	Register	Address	bit		
REGHOLD	—	3001h	[0]	0h	0: Invalid 1: Valid (Register hold)



Register Hold Setting

Mode Transitions

When changing the operating mode during sensor drive operation, set via sensor standby. However, these transitions that described below can be transitions without standby.

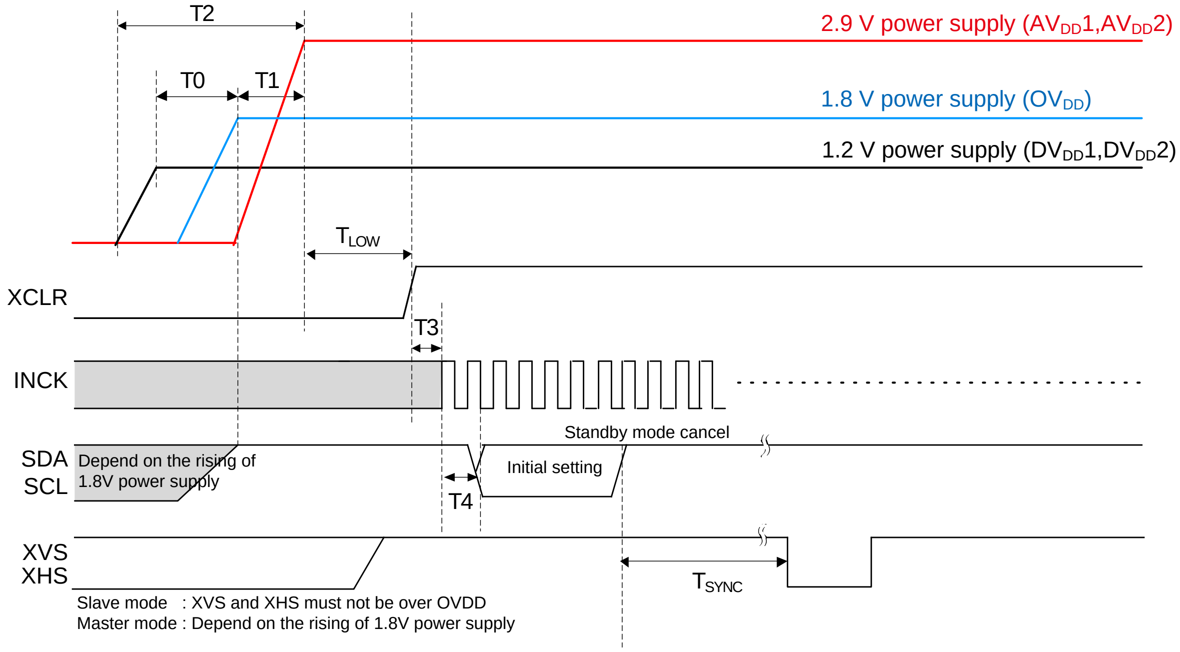
- ◆Change the number of vertical lines (In sensor master mode, change the VMAX. In sensor slave mode, change the period of XVS input.)
- ◆Horizontal and vertical scan direction. (When the vertical scan direction is changed, an invalid frame generates during transition.)
- ◆Change the mode between All-pixel scan and Window cropping. (However, It is case that transitions by not changing register HMAX . In addition, an invalid frame generates during transition.)

The changing MIPI lane setting can not support during sensor drive operation.

Power-on and Power-off Sequence

Power-on sequence

1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD1}, DV_{DD2}) →1.8 V power supply (OV_{DD}) → 2.9 V power supply (AV_{DD1}, AV_{DD12}). In addition, all power supplies should finish rising within 200 ms.
2. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.) In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}).
3. The system clear is applied by setting XCLR to High level. The maser clock input after setting the XCLR pin to High level.
4. Make the sensor setting by register communication after the system clear.

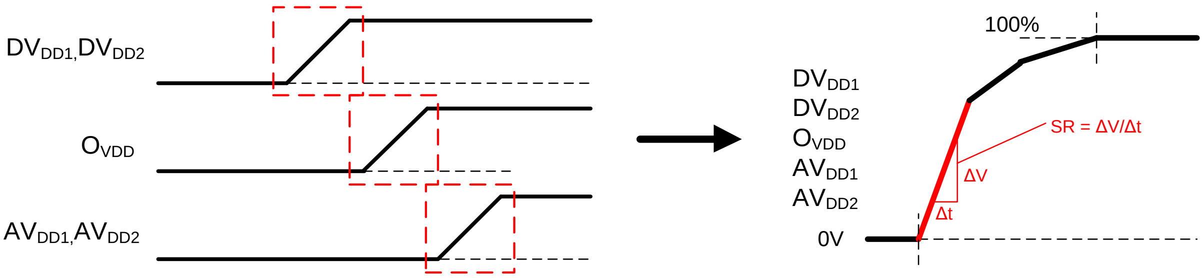


Power-on Sequence

Item	Symbol	Min.	Max.	Unit
1.2 V power supply rising → 1.8 V power supply rising	T0	0	—	ns
1.8 V power supply rising → 2.9 V power supply rising	T1	0	—	ns
Rising time of all power supply	T2	—	200	ms
2.9 V power supply rising → Clear OFF	T_{LOW}	500	—	ns
Clear OFF → INCK rising	T3	0	—	µs
Clear OFF → Communication start	T4	20	—	µs
Standby OFF (communication) → External input XHS,XVS (slave mode only)	T_{SYNC}	20	—	ms

Slew Rate Limitation of Power-on Sequence

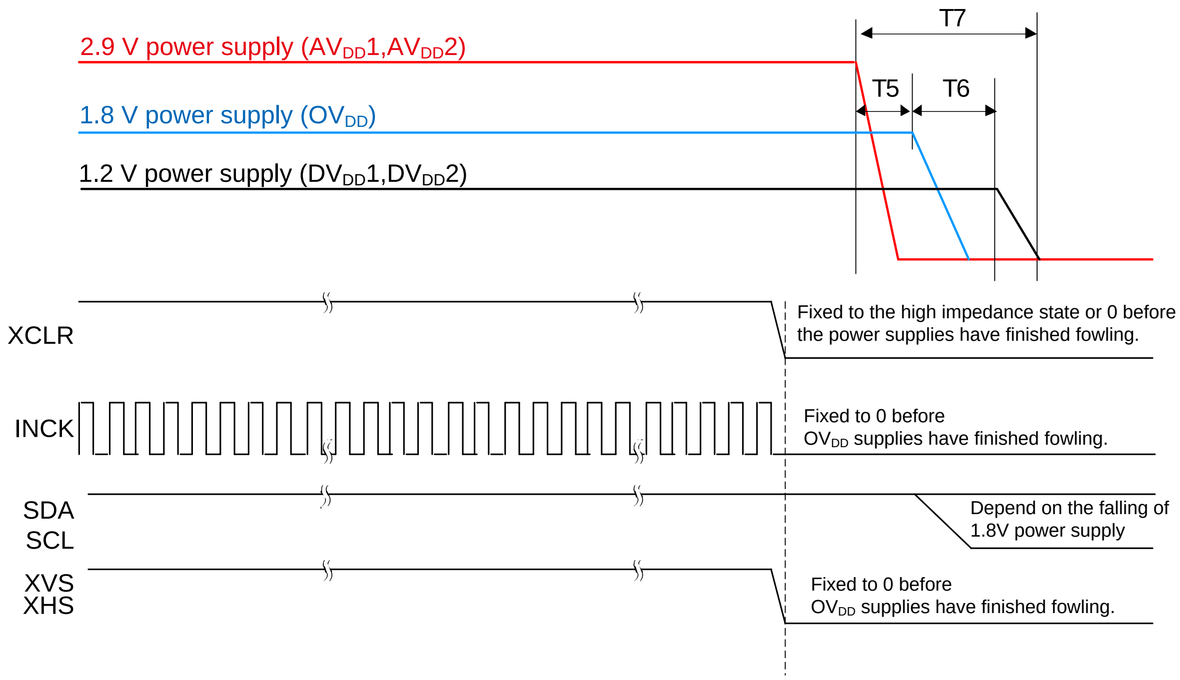
Conform the slew rate limitation shown below when power supply change 0 V to each voltage (0 % to 100 %) in power-on sequence.



Item	Symbol	Power supply	Min.	Max.	Unit	Remarks
Slew rate	SR	DV_{DD1} ,DV_{DD2}(1.2 V)	—	25	mV/µs	
		OV_{DD} (1.8 V)	—	25	mV/µs	
		AV_{DD1} ,AV_{DD2}(2.9 V)	—	25	mV/µs	

Power-off sequence

Turn Off the power supplies so that the power supplies fall in order of 2.9 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should falling within 200 ms. Set each digital input pin (INCK, SDA, SCL, XCLR, XMASTER, XVS, XHS) to 0 V before the 1.8 V power supply (OV_{DD}) falls.



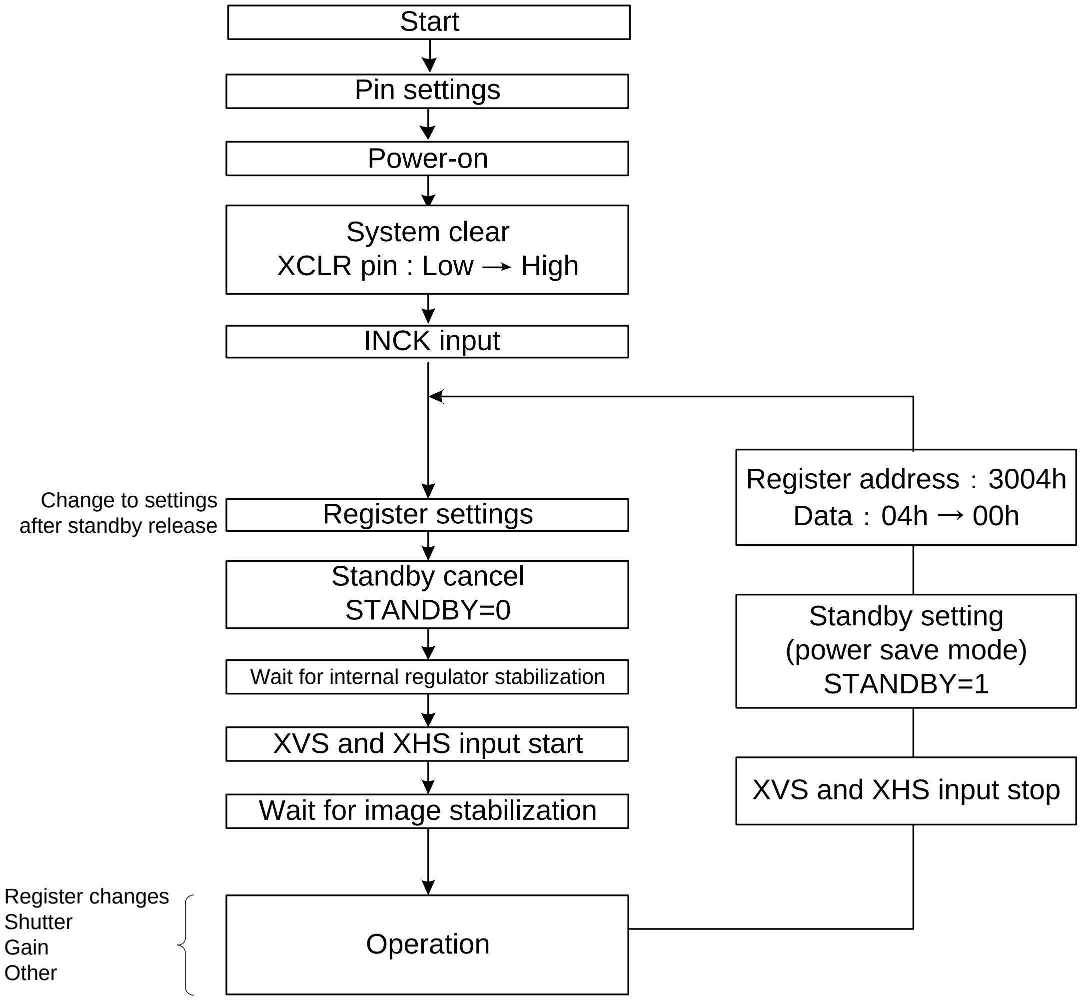
Power-off Sequence

Item	Symbol	Min.	Max.	Unit
2.9 V power shut down → 1.8 V power shut down	T5	0	—	ns
1.8 V power shut down → 1.2 V power shut down	T6	0	—	ns
Shut down time of all power supply	T7	—	200	ms

Sensor Setting Flow

Setting Flow in Sensor Slave Mode

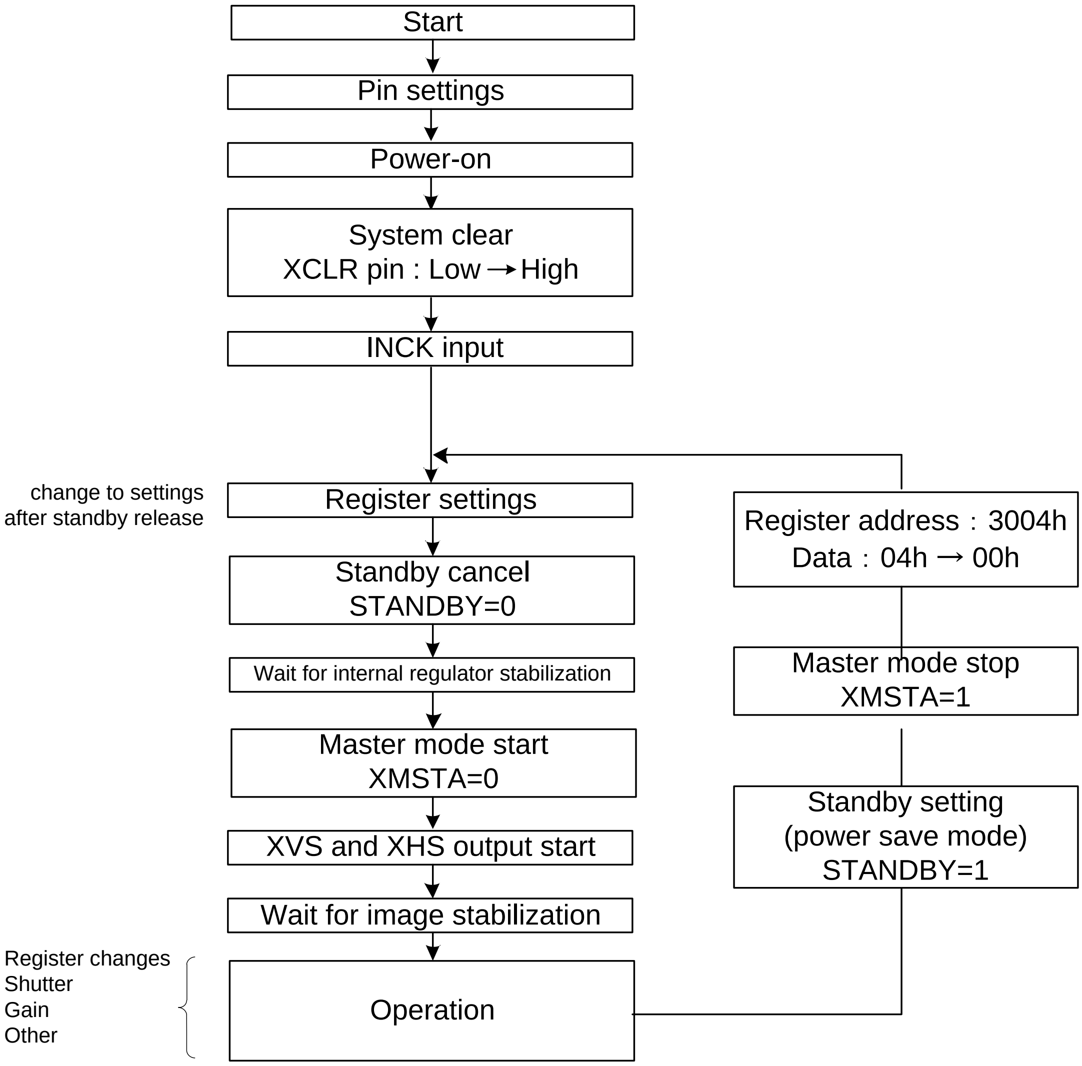
The figure below shows operating flow in sensor slave mode.
For details of "Power-on" to "Reset cancel", see the item of "Power-on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”.



Sensor Setting Flow (Sensor Slave Mode)

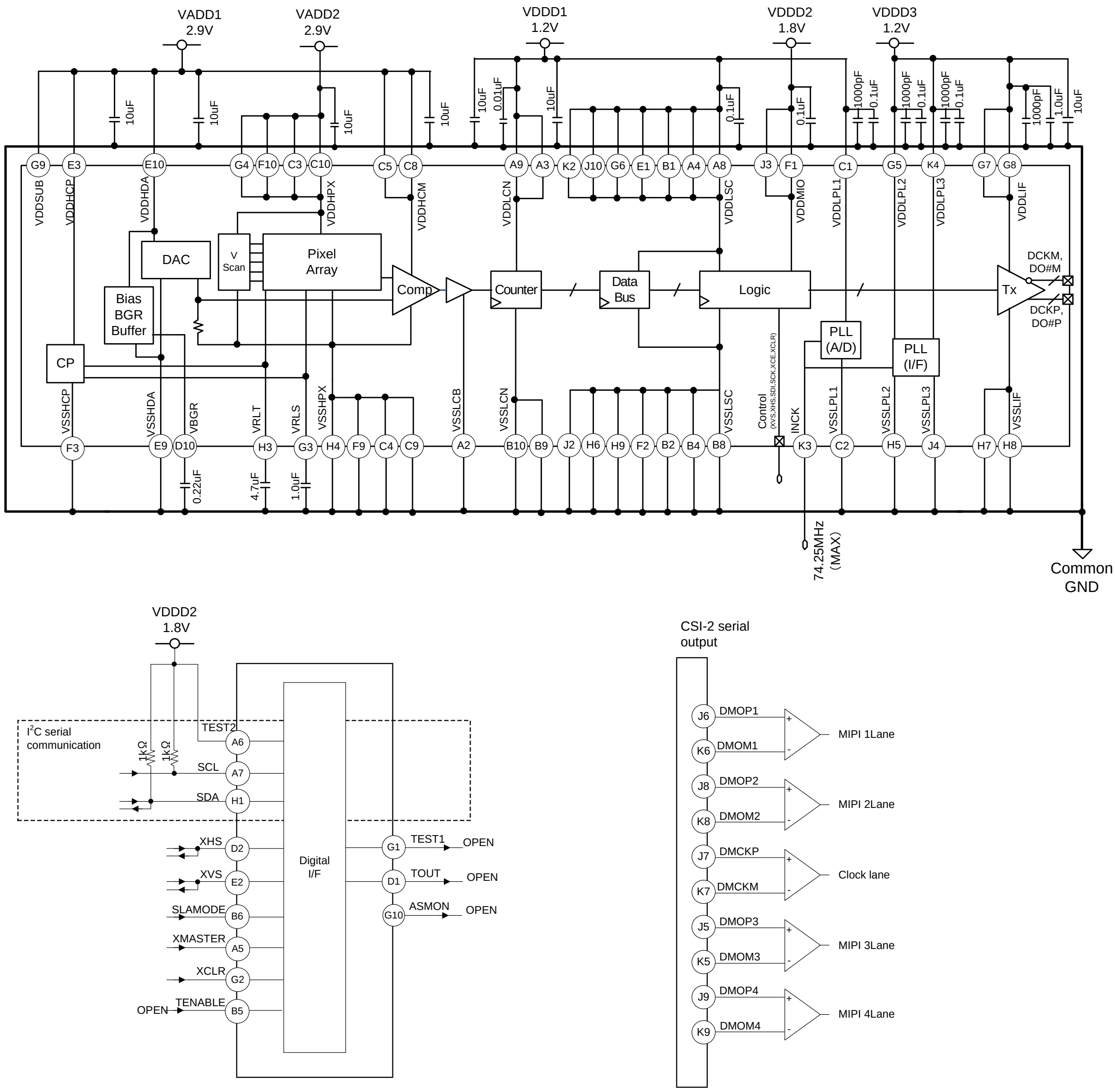
Setting Flow in Sensor Master Mode

The figure below shows operating flow in sensor master mode.
For details of "Power-on" to "Reset cancel", see the item of "Power on sequence" in this section.
For details of “Standby cancel" until "Wait for image stabilization", see the item of "Standby mode".
In master mode, “Master mode start” by setting register XMSTA to “0” after “Waiting for internal regulator stabilization”
“Standby setting (power save mode) can be made by setting the STANDBY register to “1” during “Operation”. This time, set "master mode stop" by setting XMSTA to "1".



Sensor Setting Flow (Sensor Master Mode)

Peripheral Circuit



Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Spot Pixel Specifications

(AV_{DD} = 2.9 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Tj = 60 ˚C, 30 frame/s, Gain: 0 dB)

<table>
<tr><th rowspan="2">Type of distortion</th><th rowspan="2">Level</th><th colspan="4">Maximum distorted pixels in each zone</th><th rowspan="2">Measurement method</th><th rowspan="2">Remarks</th></tr>
<tr><th>0 to II'</th><th>Effective OB</th><th>III</th><th>Ineffective OB</th></tr>
<tr><td>Black or white pixels at high light</td><td>TBD% ≤ D</td><td>TBD</td><td colspan="3">No evaluation criteria applied</td><td>1</td><td></td></tr>
<tr><td>White pixels in the dark</td><td>TBD mV ≤ D</td><td colspan="2">TBD</td><td colspan="2">No evaluation criteria applied</td><td>2</td><td>1/30 s storage</td></tr>
<tr><td>Black pixels at signal saturated</td><td>D ≤ TBD mV</td><td>TBD</td><td colspan="3">No evaluation criteria applied</td><td>3</td><td></td></tr>
</table>

Note) 1. Zone is specified based on all-pixel drive mode
2. D Spot pixel level
3. See the Spot Pixel Pattern Specifications for the specifications in which pixel and black pixel are close.

Zone Definition

TBD

Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Semiconductor Solutions Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Semiconductor Solutions Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of White Pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Tj = 60 °C / LCG mode)	Annual number of occurrence
5.6 mV or higher	TBD pcs
10.0 mV or higher	TBD pcs
24.0 mV or higher	TBD pcs
50.0 mV or higher	TBD pcs
72.0 mV or higher	TBD pcs

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

For Your Reference:

The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

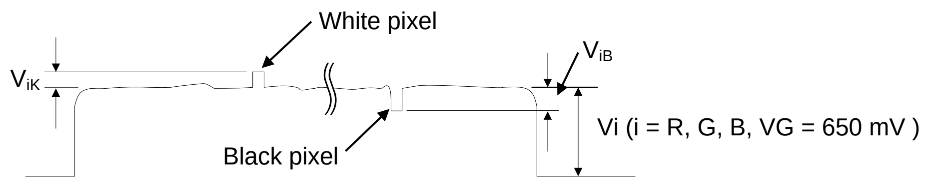
Material_No.03-0.0.9

Measurement Method for Spot Pixels

After setting to standard imaging condition II, and the device driver should be set to meet bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the luminous intensity so that the average value VG of the Gb / Gr signal outputs is 650 mV, measure the local dip point (black pixel at high light, V_{iB}) and peak point (white pixel at high light, V_{iK}) in the Gr / Gb / R / B signal output Vi (i = Gr / Gb / R / B), and substitute the value into the following formula.

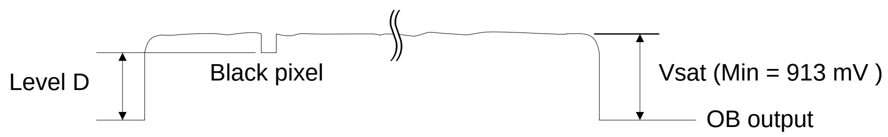
   Spot pixel level D = ((V_{iB} or V_{iK}) / Average value of Vi) × 100 [%]



Signal output waveform of R / G / B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform, using the average value of the dark signal output as a reference.

3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point, using the OB output as a reference.

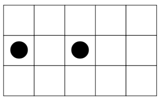
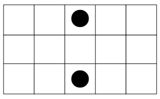


Signal output waveform of R/G/B channel

Spot Pixel Pattern Specification

White Pixel, Black Pixel and Bright Pixel are judged from the pattern whether they are allowed or rejected, and counted.

List of White Pixel, Black Pixel and Bright Pixel Pattern

No.	Pattern		White pixel Black pixel Bright pixel
No.	Pattern 	It provides by color filter array described in the left.	White pixel Black pixel Bright pixel
1		Same color	Rejected
2		Same color	Rejected

Note) 1.”●” shows the position of white pixel, black pixel and bright pixel.
White pixel, black pixel and bright pixel are specified separately according the pattern.
(Example: If a black pixel and a white pixel is in the pattern No.1 respectively, they are not judged to be rejected.)
2. When one or more spot pixels indicated “Rejected” is selected and removed.
3. Spot pixels other than described in the table above are all counted including the number of allowable spot pixels by zone.

Marking

TBD

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
(2) Use a wrist strap when handling directly.
(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
(4) Ionized air is recommended for discharge when handling image sensors.
(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).
(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)
(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.
(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package.
Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
(2) The adhesive may cause the marking on the rear surface to disappear.
(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.
(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (Reference)
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared laser for mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

TBD

(3) Others

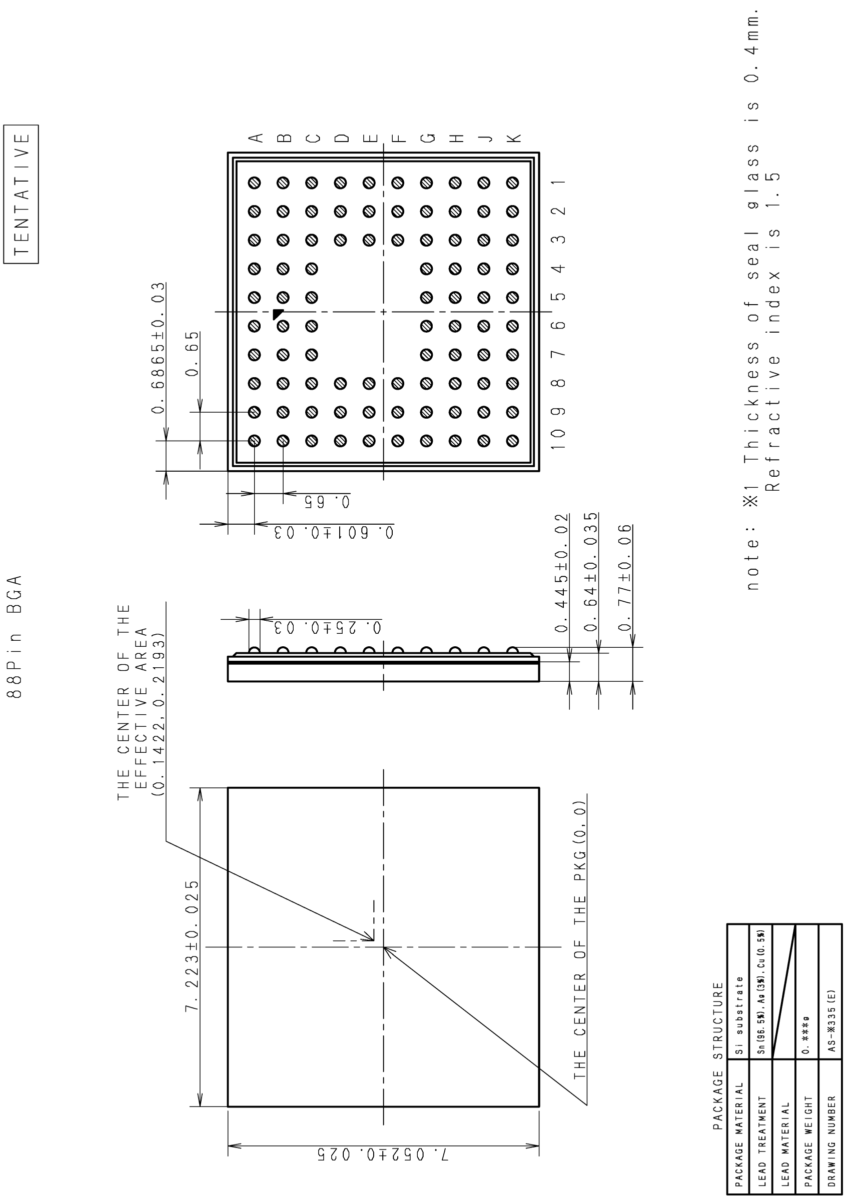
(a) Carry out evaluation for the solder joint reliability in your company.
(b) After the reflow, the paste residue of protective tape may remain around the seal glass. (The paste residue of protective tape should be ignored except remarkable one.)
(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.
(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.
(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Package Outline

(Unit: mm)



List of Trademark Logos and Definition Statements

Exmor R

* Exmor R is a trademark of Sony Corporation. The Exmor R is a Sony's CMOS image sensor with significantly enhanced imaging characteristics including sensitivity and low noise by changing fundamental structure of Exmor™ pixel adopted column parallel A/D converter to back-illuminated type.

STARVIS

* STARVIS is a trademark of Sony Corporation. The STARVIS is back-illuminated pixel technology used in CMOS image sensors for surveillance camera applications. It features a sensitivity of 2000 mV or more per 1 μm^2 (color product, when imaging with a 706 cd/m^2 light source, F5.6 in 1 s accumulation equivalent), and realizes high picture quality in the visible-light and near infrared light regions.

Revision History

Date of change	Ver	Page	Contain of Change
2017/05/22	0.1	－	First Edition
2017/06/06	0.2	7	Correction : “Optical Center” Pin No
		8	Correction : “Pixel Arrangement” Pin No
		10	Correction : “Pin Configuration”
		11-13	Correction : “Pin Description”
		24	Correction : SCL, SDA pin No
		64	Correction : “Normal and Inverted Drive Outline” Pin No
		71	Correction : “Relationship between Pin Name and MIPI Output Lane” Pin No
		80	Correction : “Peripheral Circuiti” Pin No
		88	Correction : “Package Outline” Pin No