LPDDR2 vs LPDDR3
Introduction

Contents

- DRAM Technology Comparison
- Key Functions & Features
- Power Saving Features
- Read Strobe Timing
- Other Spec

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DRAM Technology Comparison

Spec Items	DDR3	LPDDR2 - S4	LPDDR3 (S8)
Voltage (I/O and Core)	VDD=VDDQ=1.5v (1.35v)	VDD2/VDDCA/VDDQ= 1.2V VDD1= 1.8V	VDD2/VDDCA/VDDQ= 1.2V VDD1= 1.8V
Component Density	1Gb - 8Gb	64Mb - 8Gb	4Gb - 32Gb
Data rate (Mbps/pin)	800 - 2133	667 - 1066	800 - 1600
#Pre-fetch	8	4	8
# of Banks	8	8	8
Burst Length	BC4, BL8, OTF	BL4,BL8, and BL16	BL8 only
Data IO	CCT	unterminated	POD (peferred)
CMD/ADDR	unterminated	unterminated	unterminated
Strobe	Bi-directional /differential	Bi-directional /differential	Bi-directional /differential
Page size (X16/X32)	1KB for x16	1KB/2KB	1KB/2KB
Organization	X4,X8, and X16	X32(Default), X16	X32(Default), X16
Package type/balls	78/96 BGA	134/136/168/ 216/220/240 FBGA	216/256/168/253/178/346/221 FBGA

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Key Functions and Features

Functions and Features	DDR3	LPDDR2-S4	LPDDR3 (S8)
#Prefetch	8-bit	4-bit	8-bit
Command/Address Shared pin	No	Yes	Yes
TCSR (used by On-Die Temp sensor)	Yes (ASR)	Yes	Yes
Temperature Read Out	No	Yes	Yes
PASR	Yes	Yes	Yes
ODT (On Die Termination)	Yes	No	Yes
Output Driver Calibration	Yes	Yes	Yes
Read DQ training	Yes	Yes	Yes
Write leveling	Yes	No	Yes
CMD/ADDR Address Training	No	No	Yes
Deep Power down	No	Yes	Yes
Input Clock Stop and Change	No	Yes	Yes

LPDDR2/3 Pin Overview

	X32	
	LPDDR2	LPDDR3
DQ	32	32
DQS	8	8
DM	4	4
ZQ	1	1
CLK/CLK#	2	2
CS	1	1
CA0-CA9	10	10
ODT	0	1
CKE	1	1
VDD1	V	V
VDD2	V	V
VDDCA	V	V
VDDQ	V	V
VREFCA	1	1
VREFDQ	1	1
VSS	V	V
VSSCA	V	V
VSSQ	V	V
Total	61	62

New Command/Address pins :

CA0-CA9 which are shared for CMD/ADDR

Power pins separated :

VDD1 (1.8v) for core power supply1 for improving internal power efficiency

VDD2 (1.2v) core power supply2

VDDCA (1.2v) input receiver power supply

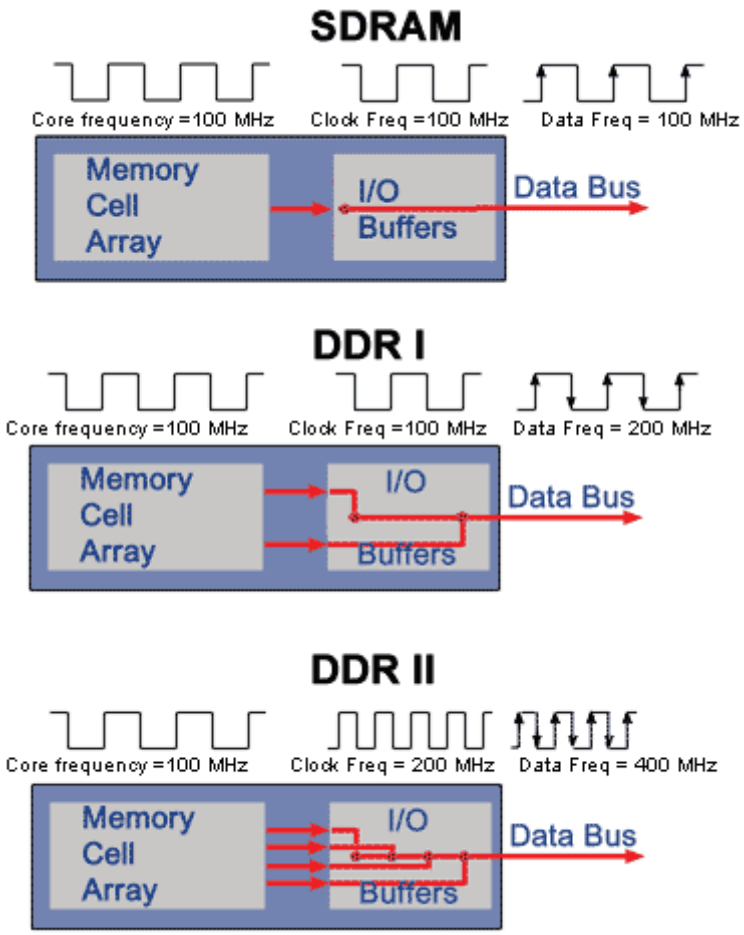
VDDQ (1.2v) IO power supply

VREFCA (0.5*VDDCA) CMD/ADDR reference voltage

VREFDQ (0.5*VDDQ) IO reference voltage

Prefetch

The LPDDR2-S4 is Prefetch 4, and LPDDR3 is Prefetch 8

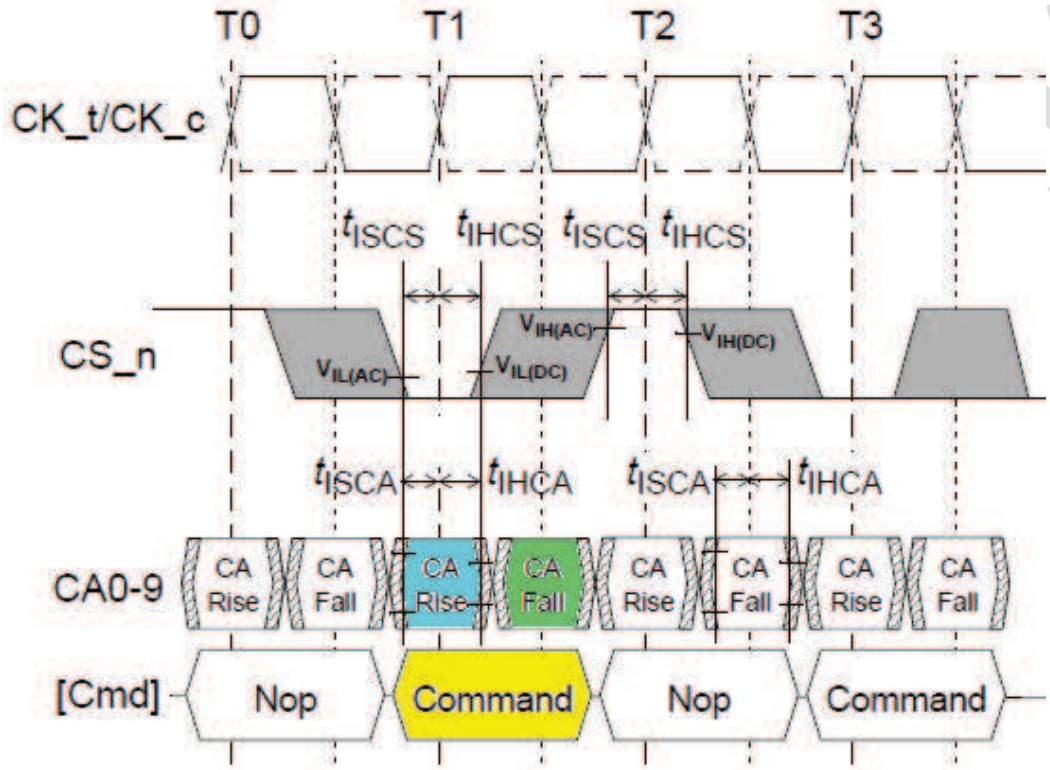


LPDDR2-S4 is prefetch 4, one column select Picks 4 bits data of one DQ from array.

LPDDR3 (S8) is prefetch 8, one column select Picks 8 bits data of one DQ from array.

Command/Address accessing timing

CA0-CA9 (CA) Command / Address inputs, some of CA pins are shared as command code



Part of command truth table :

SDRAM command	SDR Command Pins			DDR CA pins (10)										CK EDGE
	CKE		CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK_t(n-1)	CK_t(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	X								↓
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
				R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓

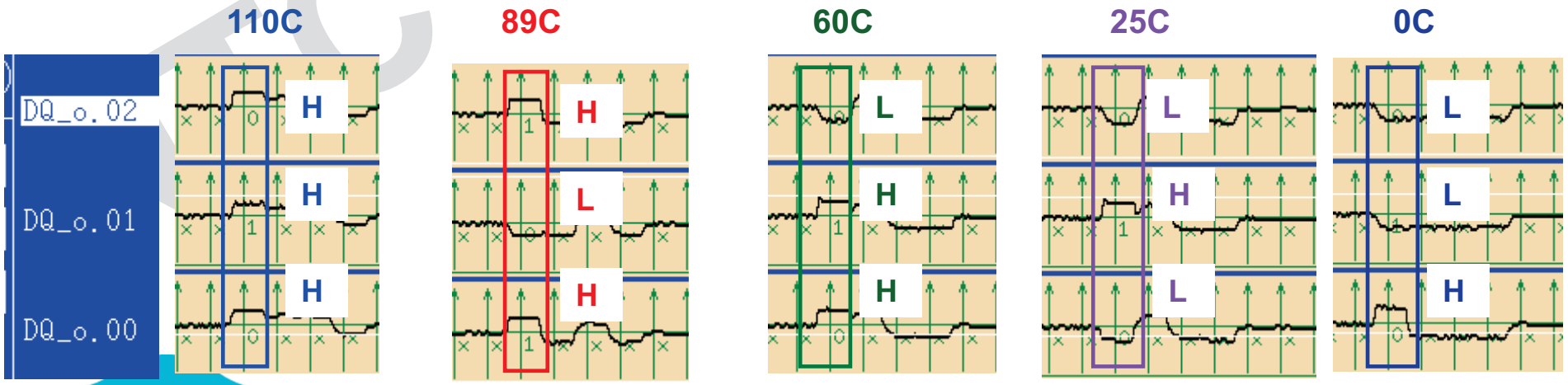
Source : JESD209-3

Temperature Read out

The LPDDR2/3 temperature can be read out via MR4 OP<2:0>

Actual Temp	Temp Read OUT via MR4
0C	001→ -40C ~0C
25C	010→ 0C ~58C
60C	011→ 58C ~85C
89C	101→ 85~106
110C	111 → >106C

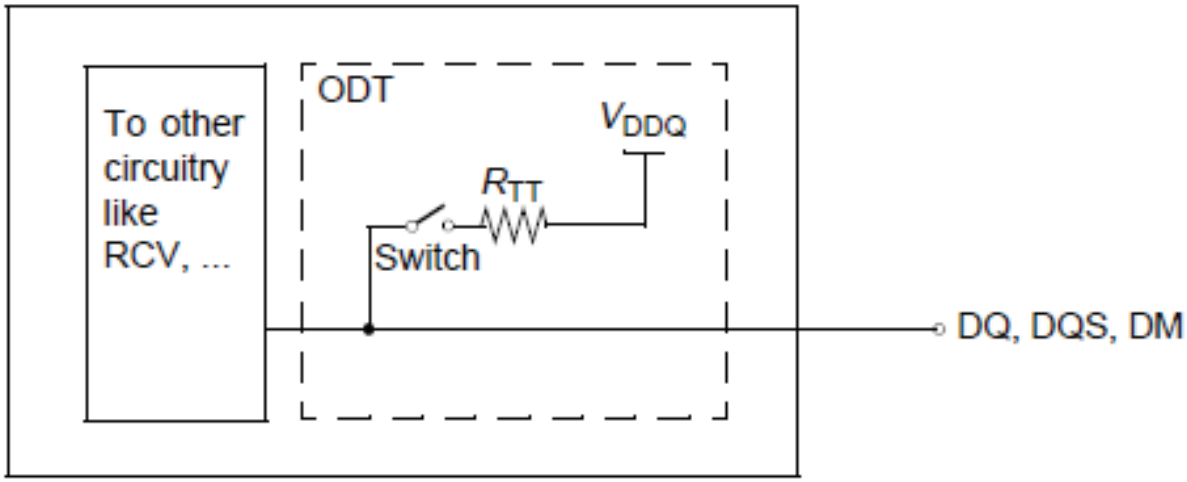
```
MP4OP<2:0>
    000   Low temp Limit          T<-40C
    001   4X tREFI                -40C<=T<0C
    010   2X tREFI                0C<=T<58C
    011   1X tREFI                58C<=T<85C
    100   N/A
    101   0.25X tREFI, No derateing   85C<=T<106C
    110   0.25X tREFI, derateing      85C<=T<106C
    111   High temp limit         T>106C
```



ODT

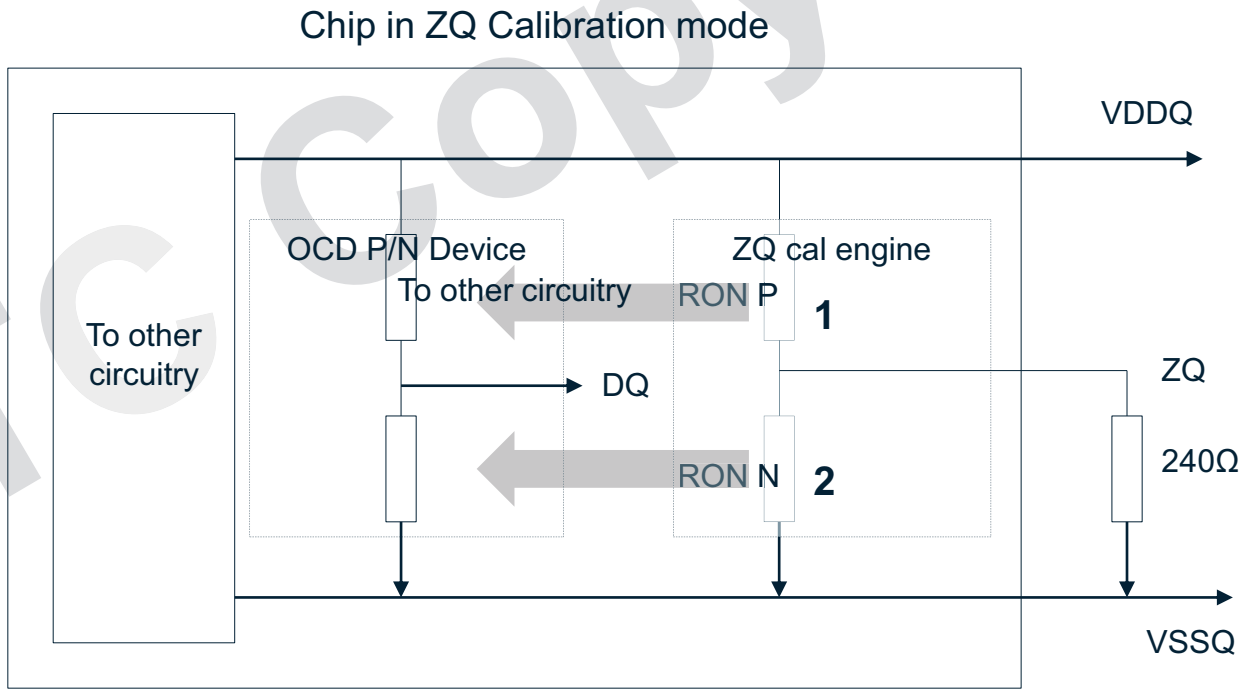
The LPDDR3 has On-Die Termination via MR11, terminate at half VDDQ , three options can be selected (ODT disable, RZQ/2 and RZQ/1 , RZQ=240Ω) for all IO, DQS, and DM pins used

LPDDR3 ODT



Output Driver Calibration

The LPDDR2/3 support ZQ calibration mode (via MR10) if ZQ is connect to VSSCA through RZQ . If ZQ is connected to VDDCA, the device operates with default calibration (ZQ Reset command must be issued, and ZQ calibration commands are ignored



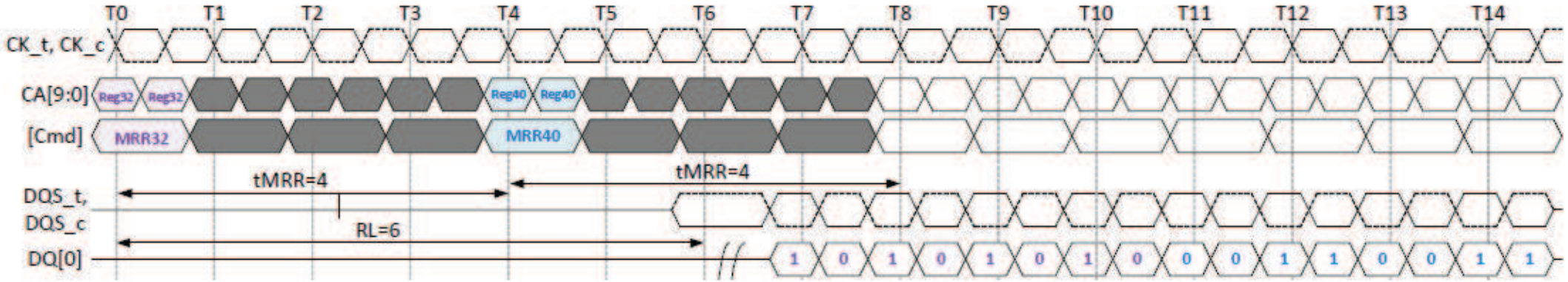
Read DQ Training

The LPDDR2/3 support DQ Calibration function for optimizing the system strobe timing, two predefined patterns can be used for this training

	LPDDR2				LPDDR3			
	Bit Time 0	**Bit Time 1**	**Bit Time 2**	**Bit Time 3**	**Bit Time 4**	**Bit Time 5**	**Bit Time 6**	**Bit Time 7**
Pattern "A" (MR32)	1	0	1	0	1	0	1	0
Pattern "B" (MR40)	0	0	1	1	0	0	1	1

High speed

Low speed

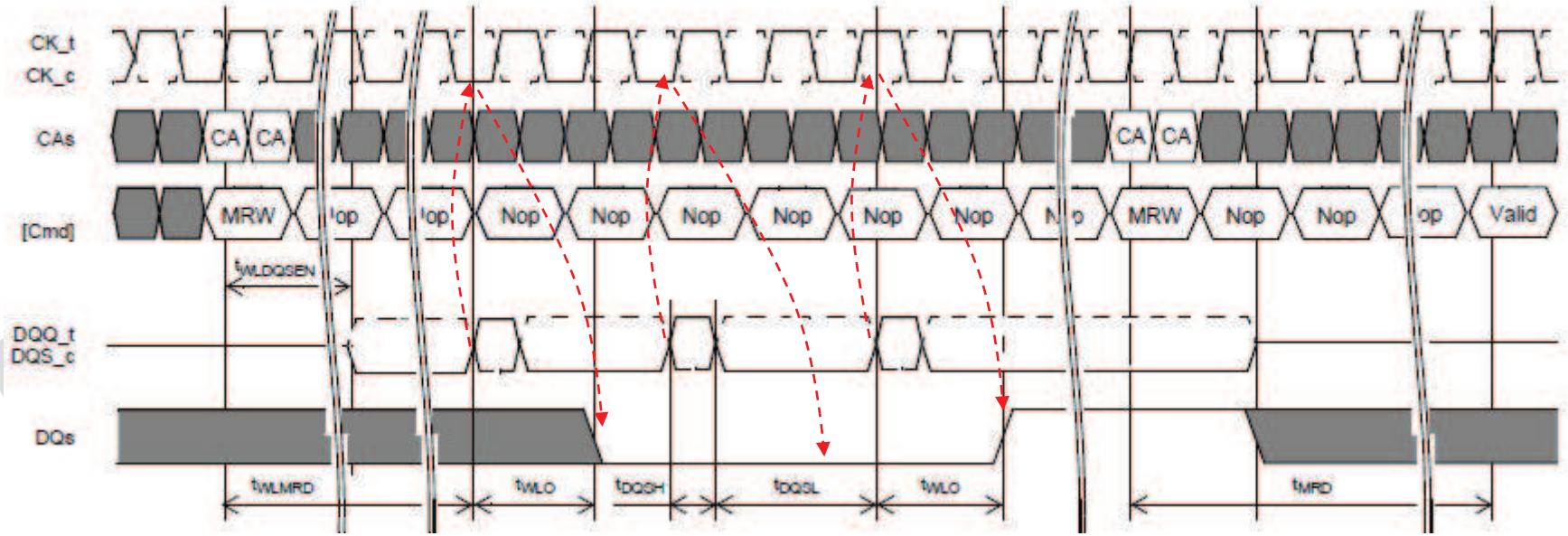


Source : JESD209-3

Write-Leveling

The LPDDR3 provides write leveling training mode for memory controller to de-skew DQS and CLK timing, DRAM samples the clock status with rising edge of DQS and provides sample result on DQ

Figure 46 — Write Leveling Timing



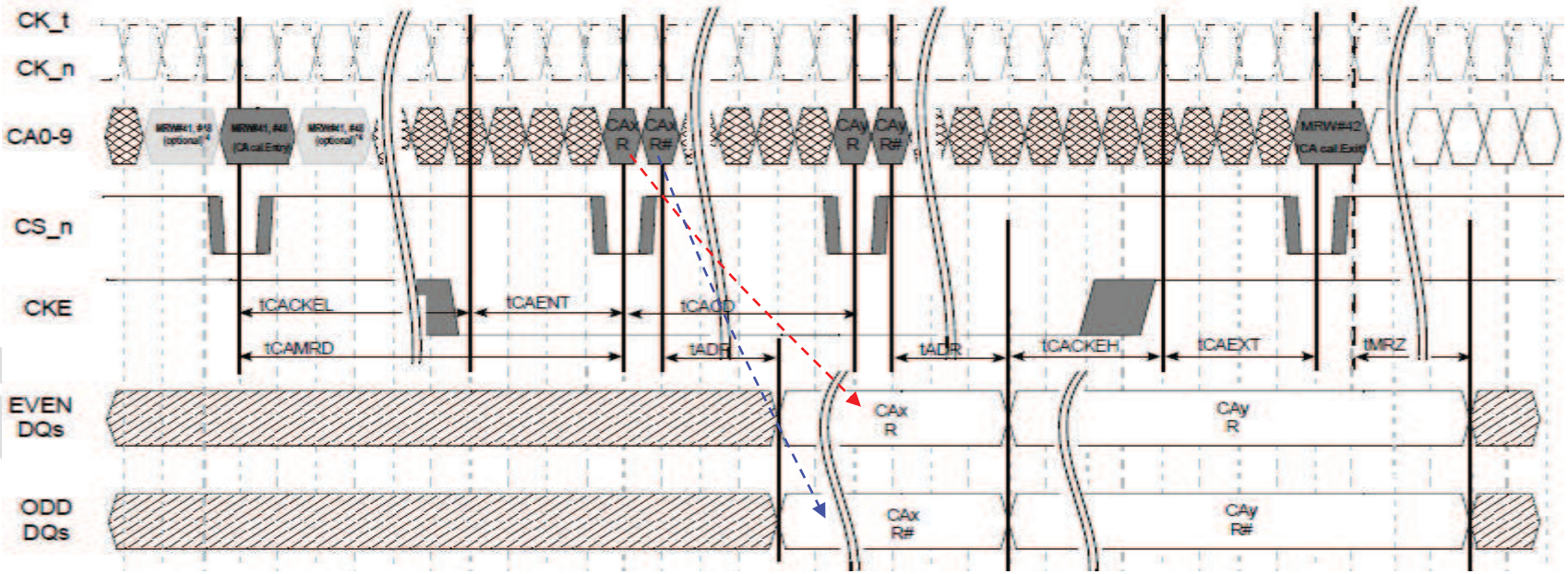
Source : JESD209-3

CMD/ADDR Training

The CA inputs operate as double data rate, it may be difficult for memory controller to satisfy CA input S/H timings at higher frequency , LPDDR3 provides CA training mode for MC adjusting CA inputs S/H timing

Seq: MRW41 for CA0-3,5-8 → MRW48 for CA4,9 →MRW 42 exit

Figure 45 — CA Training Timing chart



p.s : CKE maintains low during CA training mode

Source : JESD209-3

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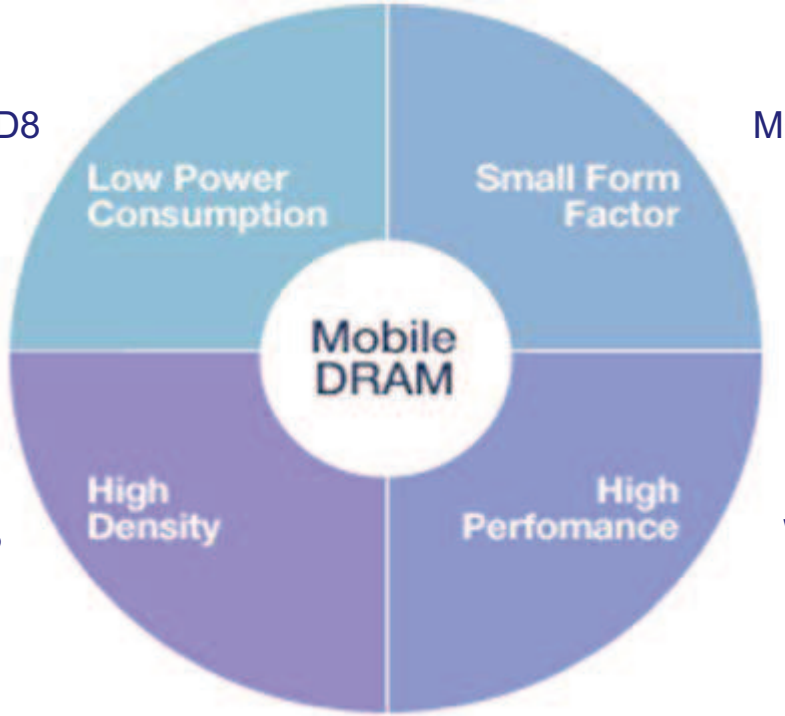
Power Saving Features

Low Power DRAM Features

Low standby current and power saving features for long battery time , such using at hand-held device as smart-phone, tablet, PDA,…

IDD2P/IDD6/IDD8

MCP,eMCP,SiP

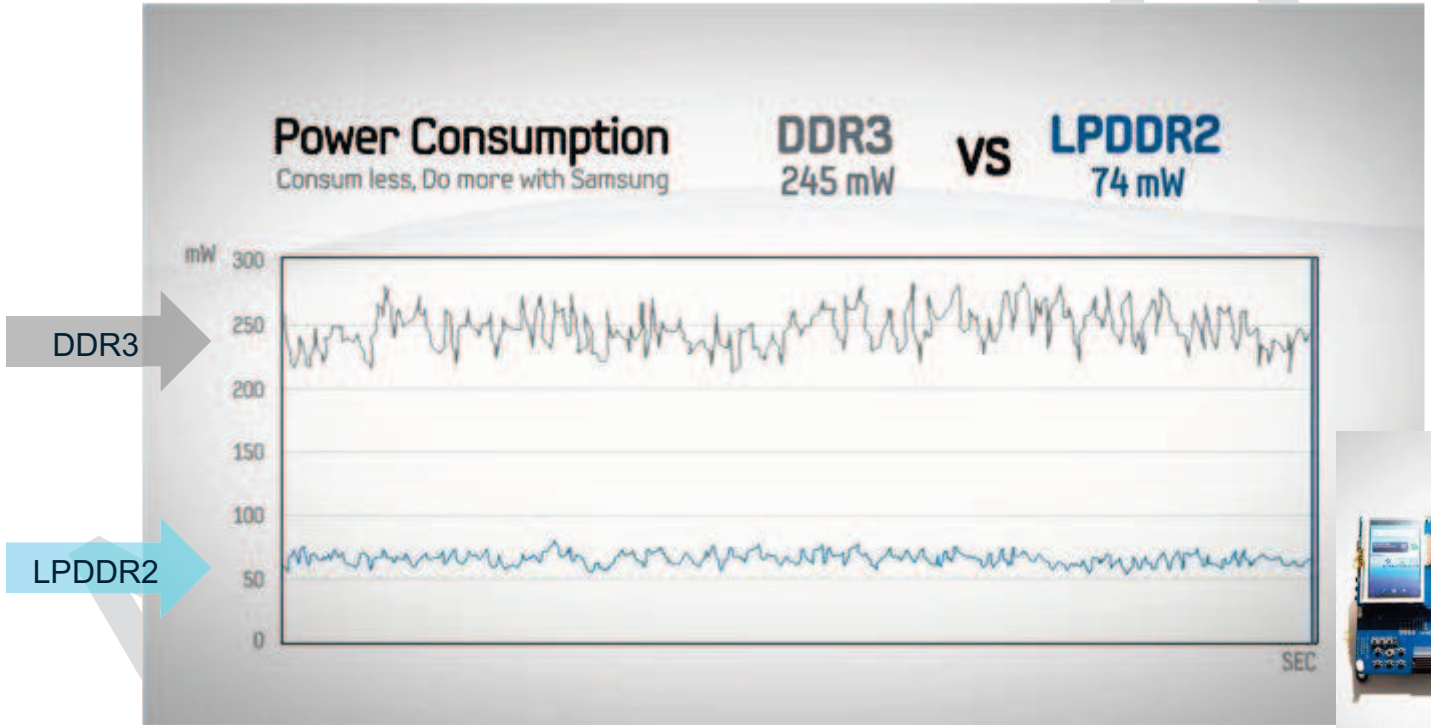


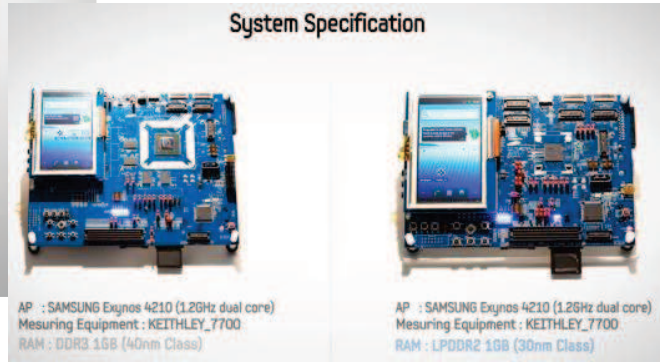
SDP,DDP,QDP

Wider IO x32,x64,…

Low Power DRAM Power Saving

LPDDR2/3 chip enables users to gain additional power savings ,the chip improves overall power efficiency at the component level up to **70%**



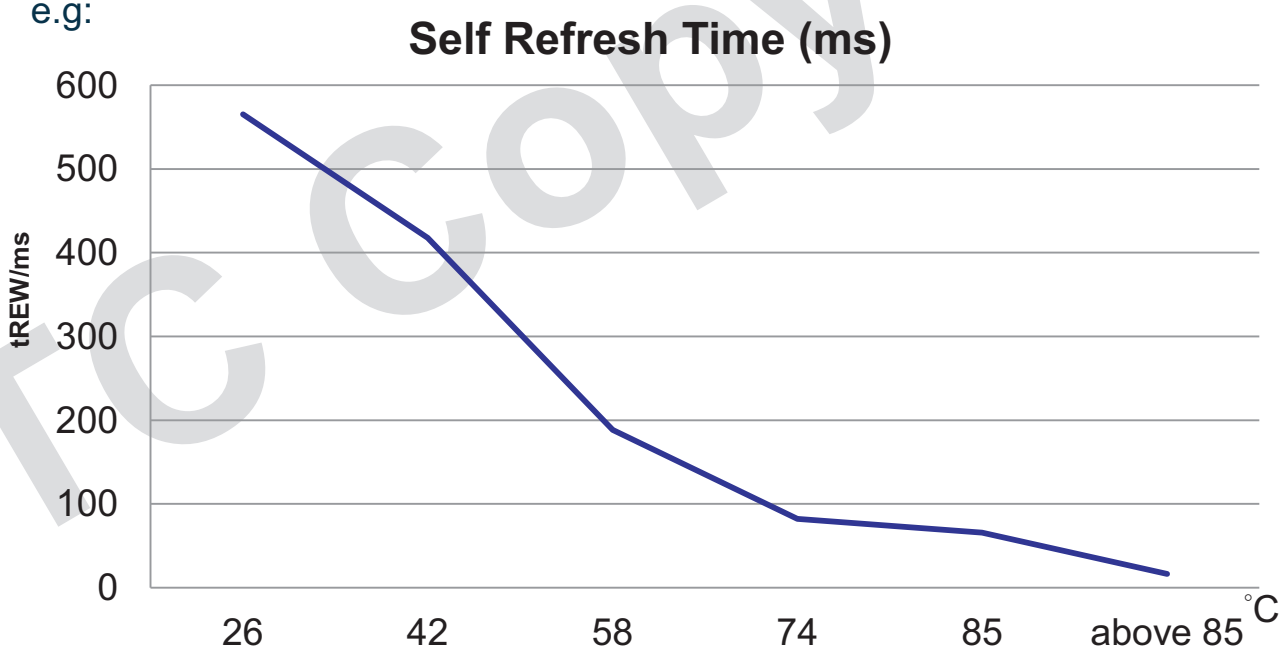


Source : film from YouTube

TCSR (Temperature Compensated Self Refresh)

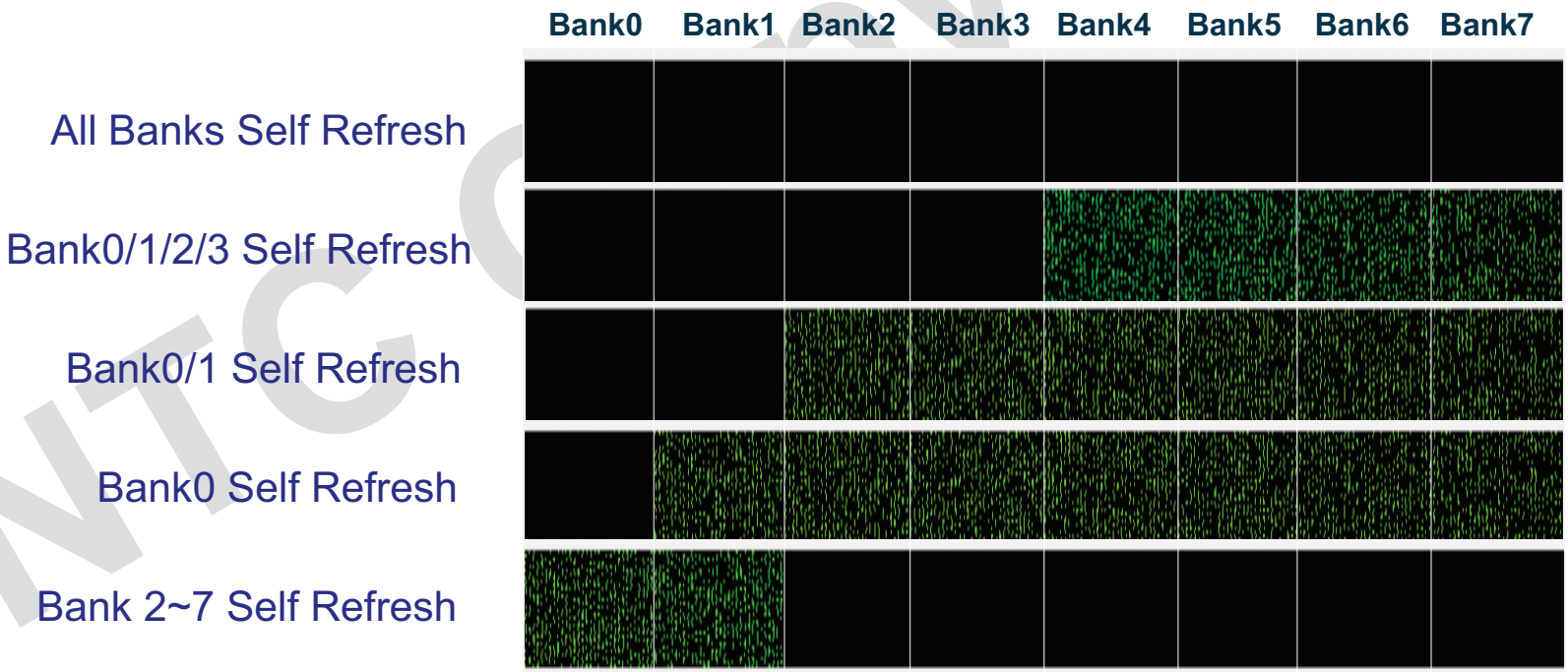
Reduced power consumption in standby mode , when the DRAM is in normal Self Refresh operation, DRAM power can be saved if the internal self refresh intervals can be adjusted for the ambient temperature .

e.g:



PASR (Partial Array Self Refresh)

When Low Power DRAM is in Self Refresh operation, if all of the array is not needed to store data, the Refresh operation can be limited to the portion of the memory's array where data will be stored .



DPD (Deep Power Down)

In some mobile applications, actual data retention in the DRAM is not required most of the time, DRAM DPD mode can turn off most or all of the on-board array voltage generators.

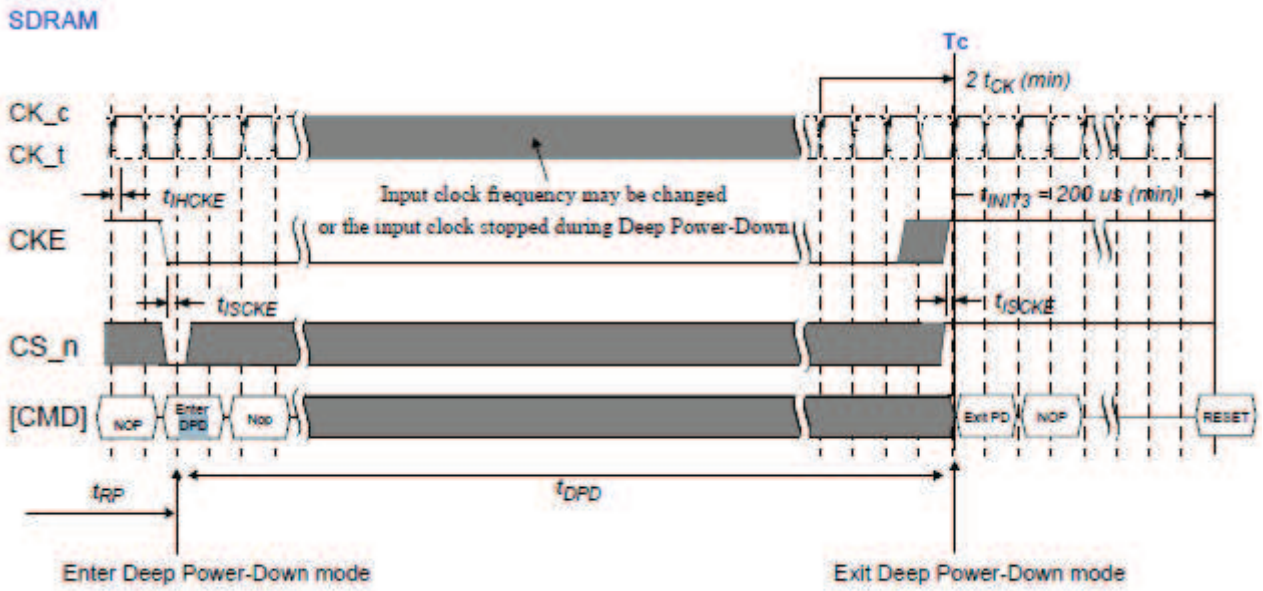


Figure 105 — LPDDR2-SX: Deep power down entry and exit timing diagram

Except CKE input buffer, all input/output buffers and internal voltages are off .

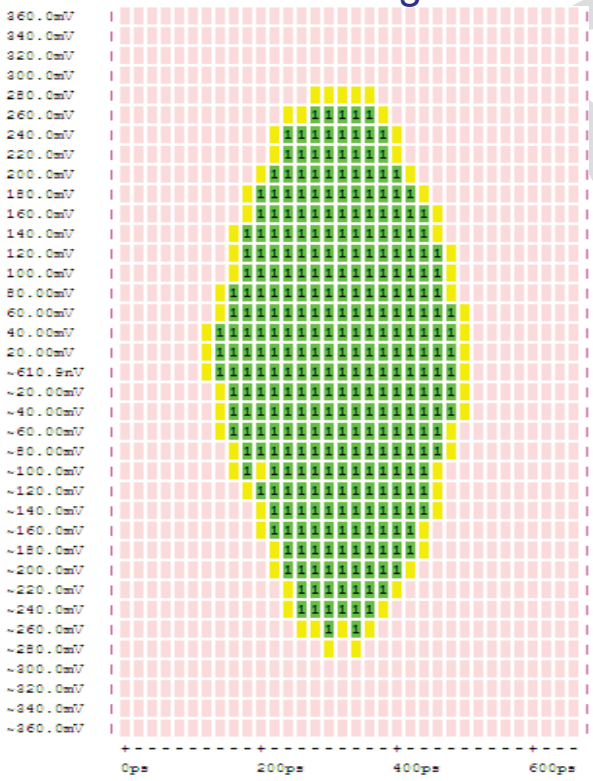
Deep power-down current (4G LPDDR2 base)	IDD8_V1	VDD1	2.5	uA
	IDD8_V2	VDD2	24.4	
	IDD8_VIN	VDDCA,VDDQ	5.26	

DS (Drive Strength)

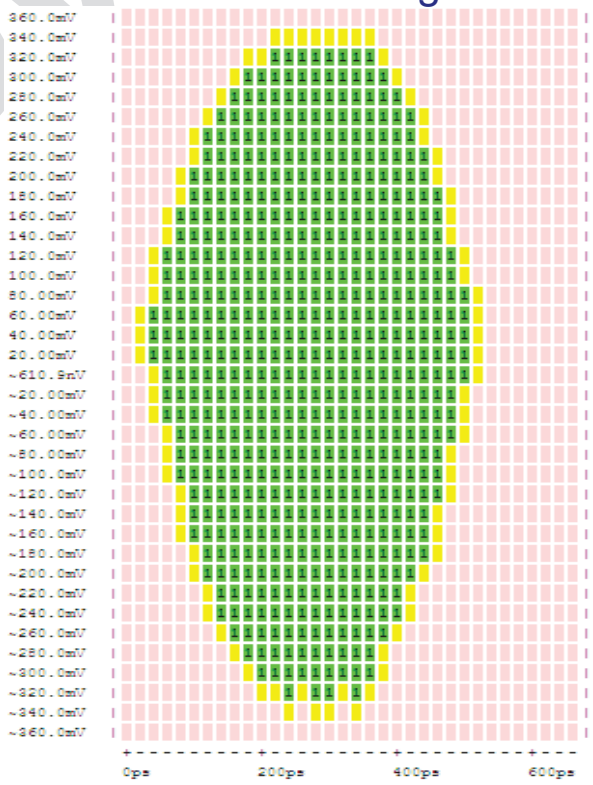
The programmable DS reduces the driver strength based on system needs, conserving energy. Programmable Drive strength (such as LPDDR1 has 1, ½ , ¼ , ¾ strength, LPDDR2/3 has 34, 40,48,60,80 ohm)

e.g. dataeye

1/2 Strength



Full Strength



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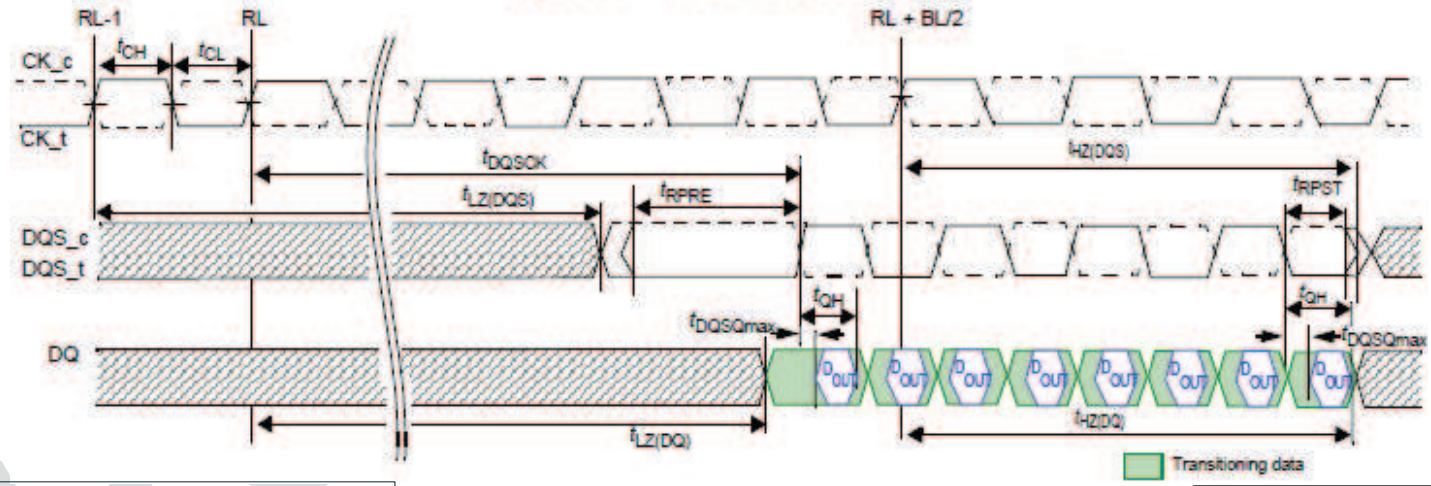
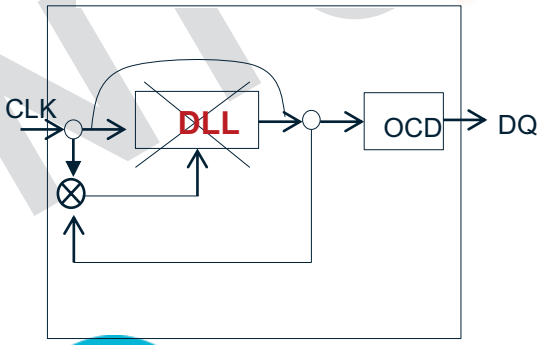
Read Strobe Timing

■ No DLL – tDQSCK drift

The LPDDR2/3 no DLL circuit design, output timing tDQSCK will drift from 2.5ns to 5.5ns , as well as tDQSCK delta timing define as below table

Figure 7 — Read Output Timing





READ Parameters[4]	Symbol	Min/ Max	Data Rate 1333	Data Rate 1600	Unit
DQS output access time from CK_t/CK_c	t_{DQSCK}	MIN	2500		ps
		MAX	5500		
DQSCK delta short[5]	$t_{DQSCKDS}$	MAX	265	220	ps
DQSCK delta medium[6]	$t_{DQSCKDM}$	MAX	593	511	ps
DQSCK delta long[7]	$t_{DQSCKDL}$	MAX	733	614	ps

Source : JESD209-3

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Other Spec

LPDDR2-S4

- Temperature range
  - Standard -25°C…+85°C
  - Extended …+105°C

same

- Input Levels
  dc = +/- 130 mV
  ac = +/- 220 mV

>>

- Ron
  uncalibrated: +/- ~30%
  calibrated +/- 15%

same

- tREFI = 3.9 μs for 4Gb and 8Gb

same

LPDDR3

- Temperature range
  - Standard -25°C…+85°C
  - Elevated …+105°C

NEW

- Input Levels
  dc = +/- 100 mV
  ac = +/- 150 mV
- Ron
  uncalibrated: +/- 30%
  calibrated +/- 15%
- tREFI = 3.9 μs for 4Gb to 16Gb

Summary

Features/Option	DDR3	LPDDR2	LPDDR3
Voltage (core and I/O)	VDD = VDDQ = 1.5V (1.35V)	VDD2/VDDCA/VDDQ= 1.2V VDD1= 1.8V	VDD2/VDDCA/VDDQ= 1.2V VDD1= 1.8V
Prefetch	8-bit	4-bit	8-bit
DLL	Yes	None	None
Data rate	800Mb/s to 2133Mb/s	667Mb/s to 1066Mb/s	800Mb/s ~ 1600Mb/s
Burst Length (BL)	4,8,OTF	4,8,16	8
Data Strobe	Differential DQS,DQS#	Differential DQS,DQS#	Differential DQS,DQS#
Banks	8	8	8
ODT (On Die Termination)	RTT: 20,30,40,60,120 Ohm via MR1	None	RTT: 120Ohm, 240Ohm via MR11
Dynamic ODT	RTT_WR: 120, 60 Ohm via MR2	None	None
DQ Driver Impedance (Ohm)	34 (Default), 40	34, 40(Default), 48, 60, 80 via MR3	34, 40(Default), 48, 60, 80 via MR3
Output Driver Calibration	ZQCL/ZQCS	None	ZQCL/ZQCS via MRW MR10
Read DQ training	Yes via MR3 MPR	Yes via MR32(PatternA), MR40(PatternB)	Yes via MR32(PatternA), MR40(PatternB)
Write leveling (for De-skews DQS and CK)	Yes	None	Yes
Input Address Training	None	None	Yes via MRW MR41/42/48
Configuration	x4,x8,X16	X32 (Default), X16	X32 (Default), X16
Deep Power down	None	Yes	Yes
TCSR (used by On-Die Temp sensor)	Yes (ASR)	Yes	Yes
PASR	Support via MR2	Support via MR16,17	Support via MR16,17

Question ?

Thanks !