H135

Cost-Effective Multimedia Platform

Overview

The H135 is an advanced application processor designed specifically for the projection market. It has a rich set of peripheral interfaces and many new features to provide a low-cost overall solution design.

Highlights

- Integrated 64-bit RISC CPU processor provides powerful computing performance.
- Supports external DDR2/DDR3/DDR3L, maximum capability up to 256 MB.
- Supports H.265/H.264 1080p@60fps video decoding, and MJPEG/JPEG 1080p@60fps video encoding.
- Rich peripheral interfaces: USB, SDIO, UART, SPI, PWM, GPADC, GPIO_ADC, IR, and so on.
- Rich video interfaces: RGB888, Dual-LVDS, and MIPI-DSI for Display.
- Important special characteristic: 1 x HDMI RX and 4-point keystone correction.

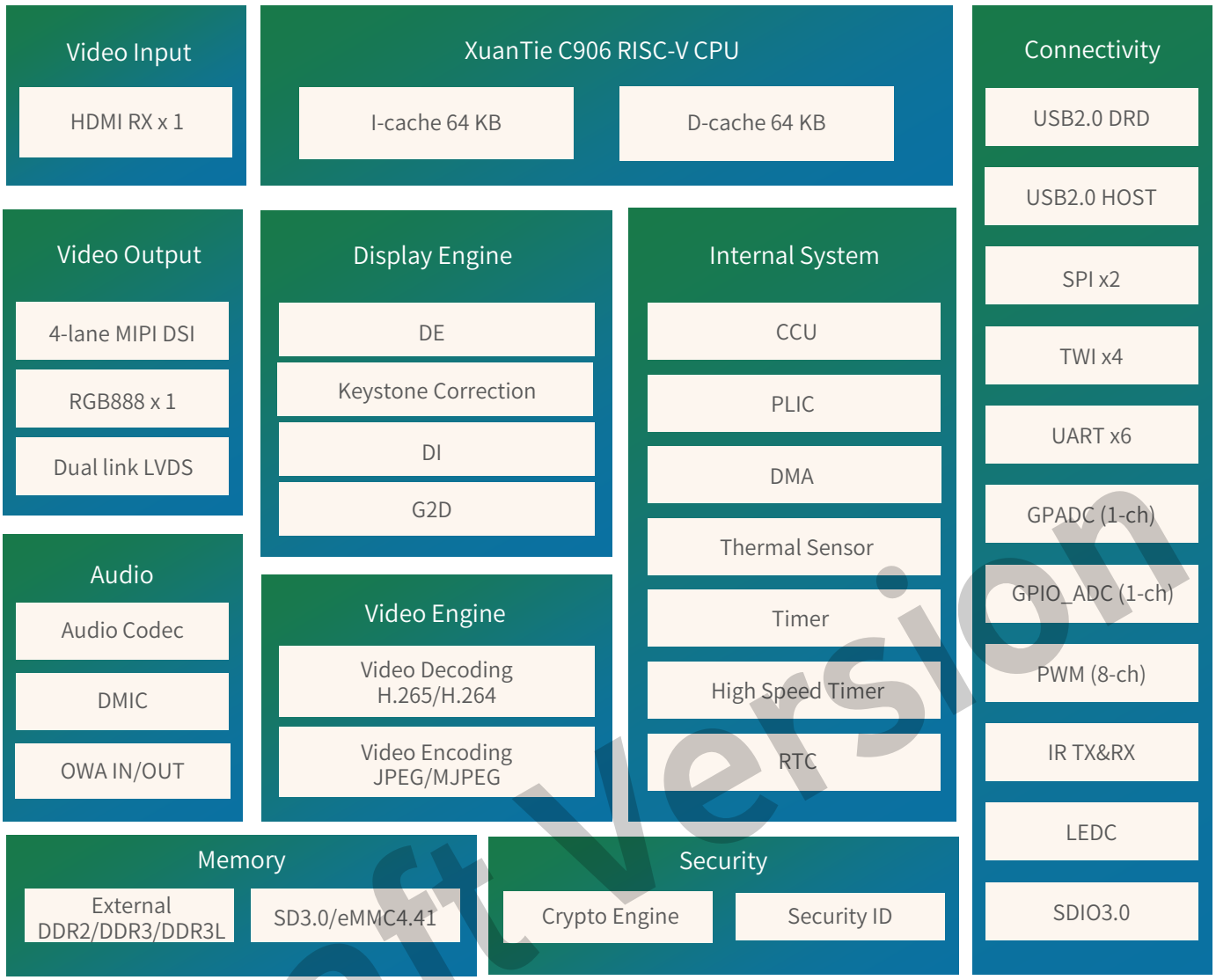
Features

CPU	• XuanTie C906 RISC-V CPU • 64 KB I-cache + 64 KB D-cache
Memory	• 16-bit DDR2/DDR3/DDR3L, maximum capability up to 256 MB • SD3.0, eMMC 4.41, SPI Nor Flash
Video Engine	• Video decoding -H.265 up to 1080p@60fps -H.264 up to 1080p@60fps -H.263, MPEG-1/2/4, VC-1, up to 1080p@60fps • Image decoding -JPEG up to 1080p@60fps • Video encoding - JPEG/MJPEG up to 1080p@60fps - Maximum resolution: 8192x8192 - Supports input picture scaling. The scaling ratio for width and height is 0.25 to 8.

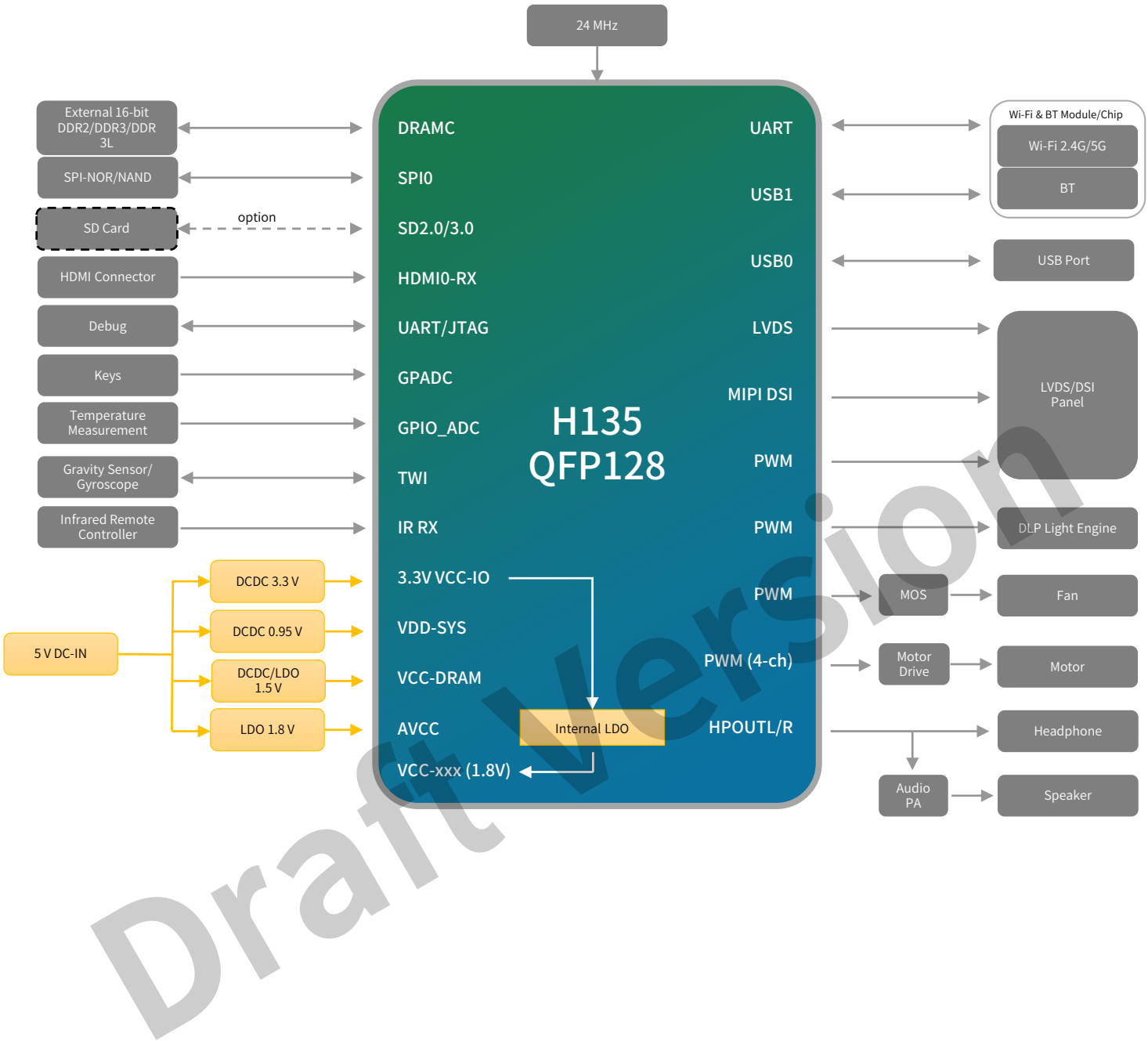
Features

Display Engine	• Allwinner Awonder1.1 Lite post processing for an excellent display experience • Supports keystone correction in online mode and [-360°,360°] rotation in offline mode • Supports de-interlace (DI) up to 1920x1080@60fps • Supports G2D hardware accelerator including rotate and mixer functions
Video OUT	• 1 x RGB888 output interface up to 1920 x 1080@60fps • Dual link LVDS interface up to 1920 x 1080@60fps • 4-lane MIPI DSI interface up to 1920 x 1200@60fps (reduced blanking)
Video IN	• 1 x HDMI RX interface - Up to 3840 x 2160 @30fps - Supports HDCP1.4 and CEC
Audio	• 2 DACs • Analog audio interfaces: HPOUTL/R • Digital audio interfaces: DMIC, OWA IN/OUT
Security	• AES, DES, 3DES encryption and decryption algorithms • RSA signature verification algorithm • MD5/SHA and HMAC tamper proofing • Hardware random number generator • Integrated 2 Kbits eFuse storage space
Connectivity	• USB2.0 DRD x 1, USB2.0 Host x 1, SPI x 2, UART x 6, TWI x 4 • PWM (8-ch), GPADC (1-ch), GPIO_ADC (1-ch, GPIO_ADC pad can be used by GPIO) • IR TX&RX, LEDC, SDIO3.0
Package	• QFP128, 14 mm x 14 mm

Block Diagram



Application Diagram



ABOUT ALLWINNER

Allwinner Technology, founded in 2007, is a outstanding designer dedicated to intelligent application SoC, high performance analog component and wireless connectivity IC. It is headquartered in Zhuhai China, with other R&D centers and offices in Shenzhen, HongKong, Xi'an, Beijing and Shanghai. Listed on the GEM of the Shenzhen Stock Exchange in 2015, with the stock code 300458.

Motivated by customer-oriented strategy, Allwinner aligns remarkable R&D teams with long-term core-technology investment in UHD video processing, high-performance multi-core CPU/GPU integration with AI and advanced manufacturing process in terms of high integration , ultra-low power consumption and full-stack integration platform, providing competitive turnkey solutions with considerate services. The products powered by Allwinner spread across from smart hardware, smart home, consumer electronics, HD media, smart video, connected car, industry control, wireless communication to analog products.

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