Data Sheet

BCM56150

24-Port Managed GbE Switch with Four GbE Uplinks, Integrated CPU, and 16 Copper PHYs

GENERAL DESCRIPTION

The Broadcom® BCM56150 System-on-a-Chip (SoC) switch family offers industry-leading integration and performance in a small footprint. The device offers up to 24 multilayer GbE ports and a maximum of four integrated 10G SerDes transceivers and associated PCS for native support of SGMII, XFI, 10GBASE-KR/CR/LR/SR with Broadcom's proprietary HiGig2™ and HiGig+ interfaces in a 29 mm x 29 mm package. Offering the industry's highest level of integration, the BCM56150 has embedded 16 GPHYs and a powerful 1 GHz ARM® Cortex™-A9 single-core processor. The BCM56150 is ideal for cost-sensitive edge connectivity applications, such as L3-managed wiring closet switches for enterprise or MTU/MDU switches for service providers.

The BCM56150 device offers multiple I/O configurations and speed (1G/2.5G/5G/10G) that address key segments of edge connectivity. A single BCM56150 device supports the popular 24x GbE switch with 4x 10GbE uplinks.

Two BCM56150 devices can be connected to build non-blocking 48x GbE switch systems with 4x 10GbE uplinks. To reduce the overall system cost, the device is engineered for low power operation to enable 48x GbE + 4x 10GbE (or 13G stacking) designs. Furthermore, the device I/O is optimized for board layout.

When used with the Broadcom QSGMII PHY, the BCM56150 device can be cascaded to the PHYs without any trace crossovers. The optimized I/O map reduces system design effort and enables low-cost PCB design.

The BCM56150 device offers many advanced features, such as IEEE 802.1Q VLAN, VLAN translation, enhanced Denial of Service (DoS) protection, IP-MAC binding checks, ARP spoofing detection, IPv4 and IPv6 support, advanced ContentAware™ Engine, IEEE 802.1p Quality of Service (QoS), Energy Efficient Ethernet™ (EEE), and HiGig™ stacking.

FEATURES

- Integrated High-Performance Cortex-A9 processor.
- Highly integrated 24-port 10/100/1000 Mbps Ethernet switch SoC.
- Embedded 16 integrated copper 10/100/1000 EEE PHYs.
- Two integrated QSGMII/1GbE interfaces.
- Up to four XFI/SFI uplink/stacking ports or 2 XFI + 2 HiGig-Duo™[13] cascade ports for non-blocking 48-port design.
- Non-blocking architecture, line rate for all packet sizes.
- Fully integrated 1.5 MB packet buffer.
- Intelligent Memory Management Unit (MMU) optimized for handling bursty data traffic.
- Advanced TCAM-based ContentAware™ Engine
- L2, IPv4/IPv6 L3 packet classification.
- Flow-based classification, metering, and marking of frames.
- Flexible Access Control List (ACL).
- Parallel lookup engines.
- Full IPv4 and IPv6 L3 routing support.
- Enhanced DoS attack statistics gathering.
- Low-power Energy Efficient Ethernet (EEE) support with Burst and Batch control policy.
- Enterprise-class L2 scalability.
- Public key acceleration (PKA) engine to support Diffie-Hellman, RSA, DSA, Elliptic Curve Diffie-Hellman (ECDH), and ECDSA for up to 4096-bit modulus size.
- Non-deterministic hardware random number generator.
- Ethernet OAM support in hardware.
- 1588 (1-step TC) support.
- 1588 Time Stamping support (2-step).
- AVB support.
- MII interface to ARM A9 for management and debug.
- Support for Industrial Temperature.
- 40 nm CMOS process.

56150-DS06-R

5300 California Avenue • Irvine, CA 92617 • Phone: 949-926-5000 • Fax: 949-926-5203

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BENEFITS

Based on industry-leading and market-proven StrataXGS® IV architecture.

Single-chip switch SoC optimized for L2 managed and light L3 Ethernet connectivity applications.

Seamless connection to StrataXGS fabric via HiGig2 protocol.

Enhanced memory technology delivers optimum usage of packet-buffer resources.

Eight flexible Class of Service (CoS) queues per port assure the lowest latency to high-priority traffic. This capability supports a wide variety of delay-sensitive video and audio multicast applications.

IPv6 support provides future-proofing.

Flow-based classification, policing, marking, and queuing deliver carrier-class SLA.

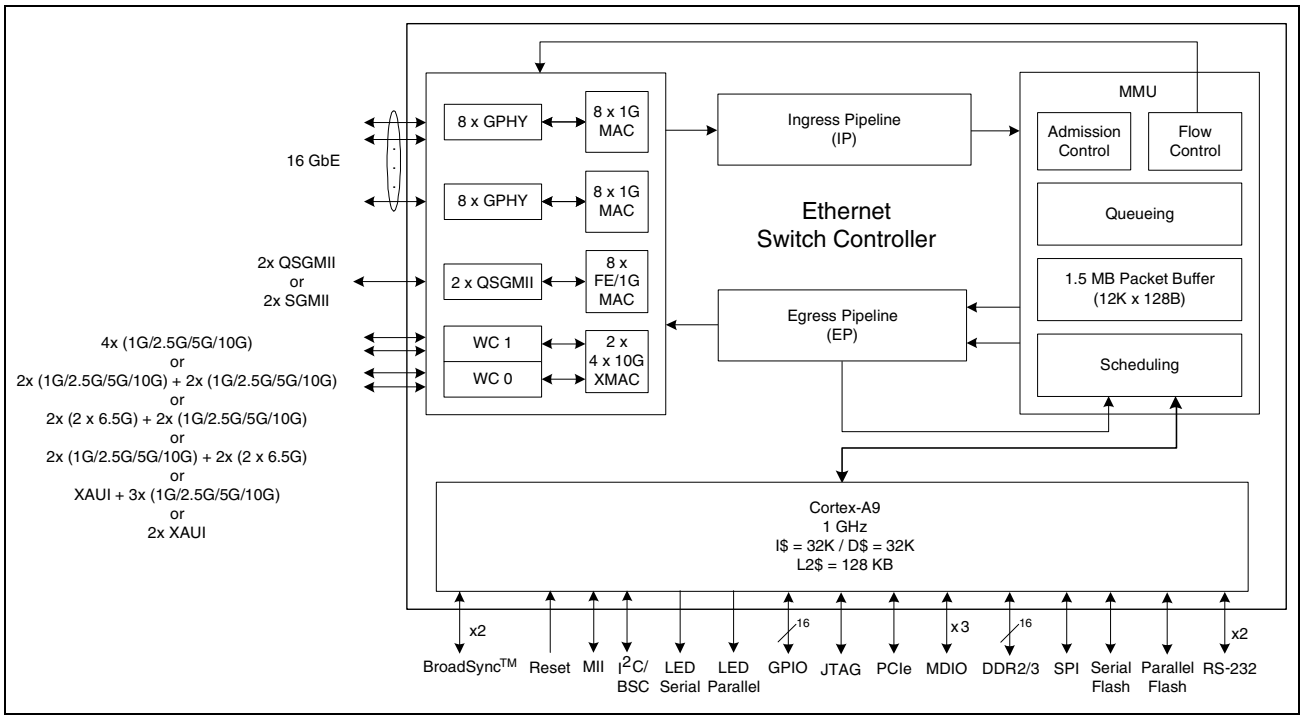
Synchronous Ethernet provides timing accuracy for delay-sensitive applications such as voce and video.

Leverages Broadcom unified API for software reuse and quick time-to-market.

Optimized ball pattern for low-cost PCB design and single-system clock source.

Low-power 40 nm CMOS technology.

Figure 1: BCM56150 Functional Block Diagram



Broadcom Corporation
5300 California Avenue
Irvine, CA 92617

Revision History

Revision	*Date*	*Change Description*
56150-DS06-R	12/11/14	Note: Page numbers referenced are valid for their respective revision of the document only. **Updated:** • Table 81: "Ordering Information for RoHS6 Devices (Contact Broadcom for Availability)," on page 166 **Added:** • Table 82: "Ordering Information for RoHS6 Devices with Exemption 15 (Eutectic Bumps Internally Between Die and Substrate)," on page 166
56150-DS05-R	07/18/14	**Updated:** • Changed Advanced Data Sheet to Data sheet. • Change Broadsync™ HD to read Broadsync™. • Change I/O of PCIE_PERST_L from O_{pu} to I_{pu}/O_{pu}. • "Power Supply Current" on page 137 - Added power column to Power Supply Current tables.
56150-DS04-R	04/07/14	**Updated:** • Figure 1: "BCM56150 Functional Block Diagram," on page 2 - Add port configurations • Table 1: "5615XCT SoC Port Configurations," on page 19 - Add port configurations • Figure 8: "Typical 5615XCT BroadScale Switching Architecture," on page 26 - Add port configurations • Table 7: "TSC Configurations," on page 47 - number of Ports Supported for Lane Speed 10.9375 increased from 1 to 4. • Changed AVS0 pin description to 'Reserved' in Table 15: "BCM5615X Hardware Signals," on page 83. • Table 18: "Pin List by Singal Name - 5615XCT Devices," on page 116 – Correct typo for pin GP2_TD2N from ball AR40 to AR4 – Correct typo for pin DNC from AL60 to AL6 • Table 21: "Operating Conditions," on page 131 - Remove 0.97V option and change 1.2V to ±3% • "Power Supply Current" on page 133 • Table 30: "BSC Signals," on page 136 – Input Low Voltage from 1.08V to 0.3*VDDO – Input High Voltage from 2.1V to 0.7*VDDO • Table 38: "MII Input Timing," on page 139 - t404 increased from 5 to 10 ns • Table 43: "SPI Slave Fast Mode Timing," on page 143 - Change t_hold from 0 to 4 ns [cont'd on next page]

Revision	Date	Change Description
56150-DS04-R continued		[cont'd from previous page] • Table 44: "MDC/MDIO Timing," on page 144 – MDC Cycle Time from 74 to 80 ns – MDIO Setup Time from 10 to 20 ns – MDIO hold time from 0 to 10 ns • Figure 36: "NAND Flash Read Cycle Timing," on page 147 - Added tRP parameter to figure • Table 49: "Default NOR Flash Read Timing," on page 150 – Change t_3 from 180 Typ. to 240 ns and t_4 from 240 Typ. to 300 ns • Table 52: "L1_RCVRD_CLK and L1_RCVRD_CLK_BKUP Output Timing," on page 154 – L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP Jitter RMS Max (12 kHz to 20 MHz) from TBD to 60 ps Max. • Table 54: "QSPI BSPI Mode Master Interface Timing Specifications," on page 155 – T_{WH} from ½T_{CK}-3 to 0.4*T_{CK} and max. 0.6*T_{CK} – T_{WL} from ½T_{CK}-3 to 0.4*T_{CK} and max. 0.6*T_{CK} – Updated footnote a • Table 55: "QSPI MSPI Mode Master Interface Timing Specifications," on page 156 – T_{WH} from ½T_{CK}-3 to 0.4*T_{CK} and max. 0.6*T_{CK} – T_{WL} from 1/0.6F_{CLK} to 0.4*T_{CK} and max. 0.6*T_{CK} – Updated footnote a • Table 61: "XTALP/XTALN Input Requirements," on page 164 – Change V_{IN} Min. from 500 to 800 $mV_{pp\ diff}$ – Change "Internal 100Ω termination" to "External 100Ω termination required • Table 62: "XG_PLL2_REFCLK Input Requirements," on page 165 – Remove Min/Max Intput Voltage V_{IL} and V_{IH} – Change V_{IN} Min. from 500 to 700 mV_{pp} diff • Table 63: "BS[1:0]_PLL_REFCLK Input Requirements," on page 166 – Remove Min/Max Intput Voltage V_{IL} and V_{IH} – Change V_{IN} Min. from 500 to 700 mV_{pp} diff • Table 64: "TS_PLL_REFCLK Input Requirements," on page 167 - Remove Min/Max Intput Voltage VIL and VIH • Table 65: "LC_PLL1_REFCLK Input Requirements," on page 168 – Remove Min/Max Intput Voltage V_{IL} and V_{IH} – Change V_{IN} Min. from 500 to 700 mV_{pp} diff [cont'd on next page]

Revision	Date	Change Description
56150-DS04-R continued		[cont'd from previous page] • Table 66: "LC_PLL0_REFCLK Input Requirements," on page 169 – Remove Min/Max Intput Voltage V_{IL} and V_{IH} – Change V_{IN} Min. from 500 to 700 mV_{pp} diff • Table 67: "EXT_QS2_CLKP/N Output Specifications," on page 170 – Change V_{ODIFF} Min from 500 to 300 mV_{pp} diff and Max from 2000 to 500 mV_{pp} diff – Remove Min/Max Output Voltage V_{OL} and V_{OH} – Change EXT_QS2_CLK Rise/Fall time from 1.0 to 0.22 ns Max. – Change EXT_QS2_CLK jitter from 0.5 to 2 ps Max. – Remove Note: Internal 100Ω termination – Measured with 50 termination as recommended in the Hardware Design Guide • Table 68: "BS[1:0]_PLL_CLK Output Specifications," on page 171 • Typical BS[1:0]_PLL_CLK Frequency to (20 Mhz, 25 MHz, 125 MHz, 156.25 MHZ) • Remove Note: Internal 100Ω termination • Change V_{ODIFF} Min from 500 to 300 mVpp diff and Max from 2000 to 500 mVpp diff • Change "Input Voltage Range" to "Output Voltage Range" • Remove Minimum Input Voltage • Remove Maximum Input Voltage • Change BS[1:0]_PLL_CLK Rise/Fall time from 1.0 to 0.22 ns Max. • Add jitters for 20, 25, 125 and 156.25 MHz • Measured with 50Ω termination as recommended in the Hardware Design Guide • Table 76: "Serial Interface Receive Characteristics," on page 177 - tskewi Max. from 0.23 to TBD • Table 77: "Serial Interface Transmit Characteristics," on page 178 • t_{fall} Min. from 2 to 24 • t_{rise} Min. from 2 to 24 • delta-t_{TXWDM} Max. from 0.17 to TBD • Table 82: "AC-JTAG Transmit Setting (Driver Bias Current)," on page 181 - the Transmit Amplitude of the entire table. • Section 9: "Thermal Characteristics," on page 182 [cont'd on next page]

Revision	*Date*	*Change Description*
56150-DS04-R continued		[cont'd from previous page] **Added:** • "DDR3 Interface AC Specifications" on page 157 • A Note to "IEEE 1588" on page 60 **Removed:** • QS0_PVDD and QS1_PVDD in Table 15: "BCM5615X Hardware Signals," on page 83 • Hardware strapping pin description to enable Super Isolate Mode.
56150-DS03-R	07/03/13	**Updated:** • Updated entire document. • Table 1: "5615X_5333X_5334XCT SoC Port Configurations," on page 14 • For power sequencing add requirement to power up the core VDDC at the same time or before GP-AVDDL SUPPLY. • Table 2: "Switch Features," on page 29 - Adjust table sizes. • Add PU/PD
56150-DS02-R	01/10/13	Updated entire document.
56150-DS01-R	12/21/12	Updated entire document.
56150-DS00-R	08/08/12	Initial release

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About This Document

Purpose and Audience

This document describes the Broadcom® BCM56150 System on Chip (SoC). The Broadcom BCM56150 integrates a high-performance 1 GHz ARM Cortex-A9 processor and an Ethernet Switch controller with 24 multilayer GbE ports and up to four configurable XFI ports. This document is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

Acronyms and abbreviations in this document are also defined in Appendix A: “Acronyms and Abbreviations,” on page 167.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads and Support site (http://www.broadcom.com/support/).

Section 1: Introduction

Note: This is an Advanced Data Sheet; information presented in this document, including parameters, may change.

Overview

The Broadcom BCM56150 is a System on Chip (SoC) optimized for power and cost without compromising performance. The BCM56150 integrates:

- A high-performance 1 GHz ARM Cortex-A9 processor.
- An Ethernet Switch controller with 24 multilayer GbE ports.
- Two QSGMII interfaces.
- Two TSC ports with flexible configuration as shown in Table 1.
- Up to 16 GbE transceivers.

The Broadcom BCM56150 SoC port configurations are shown in Table 1.

Table 1: *BCM56150 SoC Port Configurations*

Device	*GbE Port*	*QSGMII*	*TSC 1*	*TSC 0*	*L3 Features*	*L2 Features*
BCM56150	16	2x QSGMII/ 2x SGMII	–	4x 1G/2.5G/5G/10G	Yes	Yes
			2x 1G/2.5G/5G/10G	2x 1G/2.5G/5G/10G		
			4x 1G/2.5G/5G/10G	–		
			2x HiGig Duo [13]	2x 1G/2.5G/5G/10G		
			2x 1G/2.5G/5G/10G	2x HiGig Duo [13]		
			XAUI	3x 1G/2.5G/5G/10G		
			XAUI	XAUI		

Ethernet Switch Controller

The Broadcom® BCM56150 integrates 16 GbE ports with embedded GPHYs and 8 GbE ports through QSGMII interfaces and two TSC ports with flexible configuration as shown in Table 1 on page 19.

The BCM56150 is a highly integrated solution ideally suited for stand-alone GbE switches as well as stackable GbE switches. The switch controller combines all the functions of a high-speed switch system, including packet buffer, SerDes, media access controllers, address management, and a non-blocking switch fabric. The BCM56150 device supports auto-DoS attack prevention and SNMP, IEEE 802.1x, Spanning Tree, and Rapid Spanning Tree protocols.

The BCM56150:

- Provides 16 full-duplex GbE ports with embedded GPHYs.
- Provides two QSGMII interface to external PHYs for additional eight full-duplex GbE ports. These GbE ports support both copper and fiber media (via external PHY device).
- Provides four stackable/uplink 10G ports.
- Supports 48-port GbE + four 10GbE non-blocking L3 switch design, using two BCM56150 devices.
- Integrates 1.5 MB internal memory in the Common Buffer Pool (CBP) for packet buffering.
- Provides hardware support for IPv4 and IPv6 protocols.
- Supports a Broadcom Serial control (BSC) controller for communicating with external devices such as serial EEPROM, and Flash ROM devices.
- Supports a serial interface for the MII management (MDC/MDIO) of physical layer devices.
- Supports PCIe interface for external CPU host communication.
- Contains the memory needed to host L2 and L3 switching tables.
- Supports VLAN double-tagging.
- Supports advanced QoS shaping for service provider networks.
- ContentAware™ processing (via the Filter Processor (FP) feature) enables unmatched flexibility and programmability. The ContentAware engine can be used for applications such as policy-based routing or Access Control List (ACL) operation.
- Integrates sophisticated metering, statistics, and traffic management features, optimizing the QoS for voice, video, and data convergence.
- Provides built-in security functions for highly secure enterprise network.

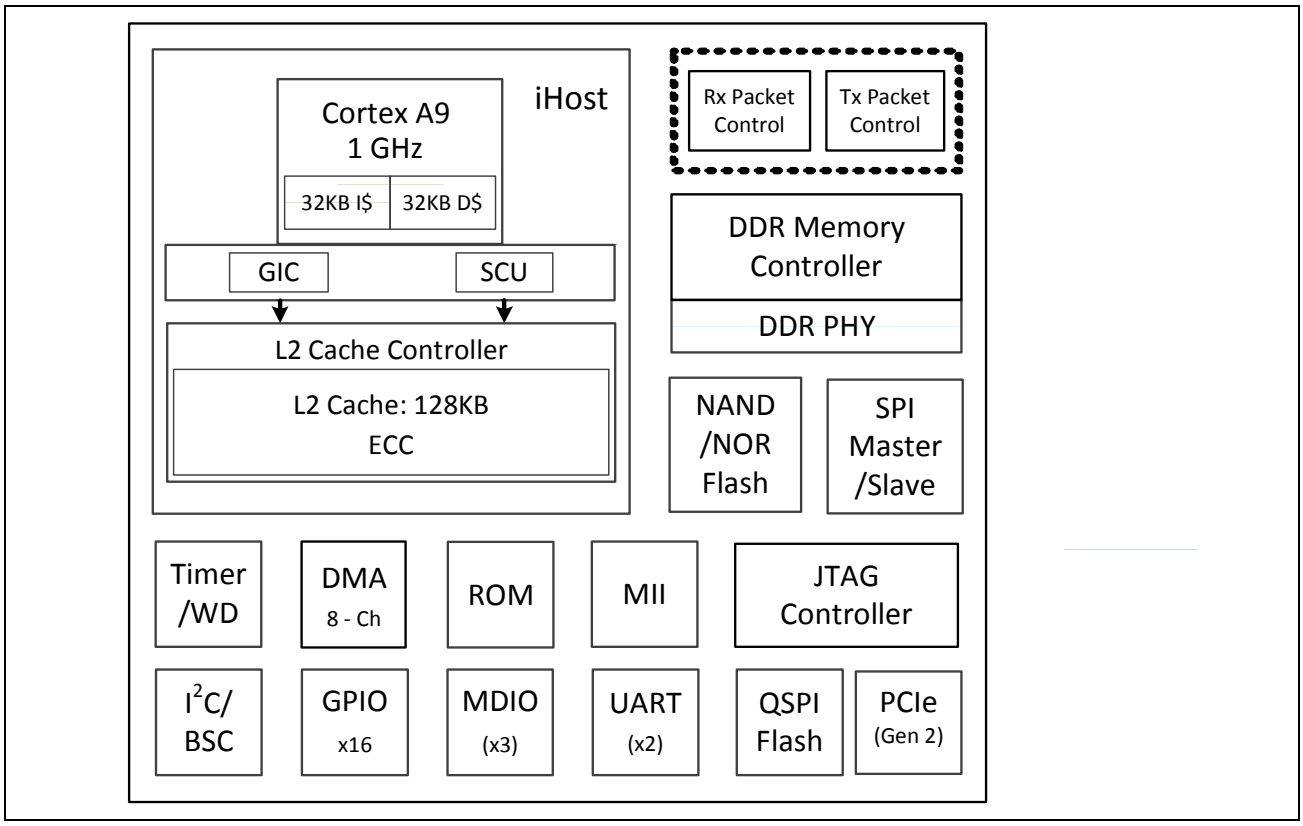
ARM Cortex-A9 Processor

The BCM56150 Integrates a high-performance 1 GHz ARM Cortex-A9 processor with a 32 KB four-way set associative instruction cache, a 32 KB four-way set associative data cache, and a 128 KB L2 cache. The Cortex-A9 processor offers significant performance improvements in both transfer rates and CPU utilization.

The BCM56150 provides flexible support for a variety of system bus interfaces, including PCI Express Gen-2 (X1 lane), 16-bit DDR2-800 MT/s or DDR3-1333 MT/s memory controller, serial and NAND as well as NOR Flash port. There are up to 16 GPIOs on the Cortex-A9 processor. All inputs are capable of generating processor interrupts.

- Cortex-A9
- Maximum CPU speed 1 GHz
- 32 KB 4-way set associative I-cache and D-cache
- 128K L2 cache
- 128-entry TLB
- 16-bit DDR2-800 MT/DDR3-1333 MT memory controller
- 1 port PCIe 2.0, one lane
- Serial and parallel flash ports
- 1 port BSC
- 2 UART port
- 16 GPIOs
- 3 separate MDIO interfaces
- 1 SPI port

Figure 2: BCM56150 Embedded Processor Functional Block Diagram

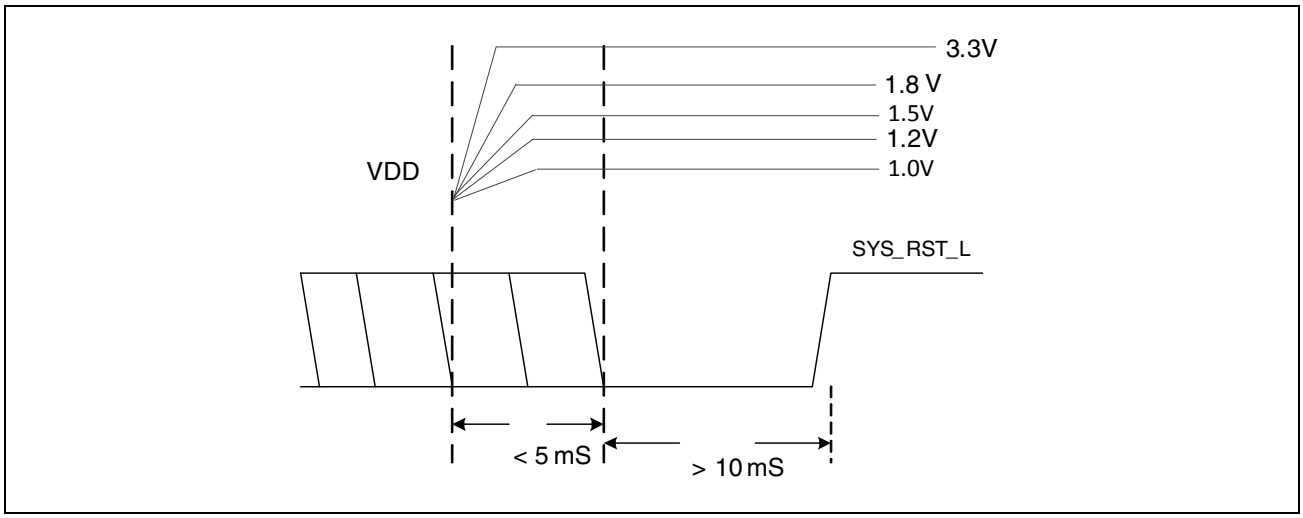


Section 2: Common Interfaces

System Reset

Upon system power-up, the device internal logic will stay in reset for roughly 5 ms. The power-up state is achieved when 1.0V, 1.2V, 1.5V, 1.8V, and 3.3V are at steady state voltage. It is recommended that the user asserts SYS_RST_L for at least 40 ms after the voltages are stable. Most external Power-on-Reset (POR) devices will properly keep the reset signal low immediately from power-on until the power supply is stable. When using an FPGA/CPLD to drive the reset, a pull-down resistor may be required to ensure the SYS_RST_L signal is low. Figure 3 illustrates the reset sequence relative to the ramping power supplies.

Figure 3: System Reset Sequence



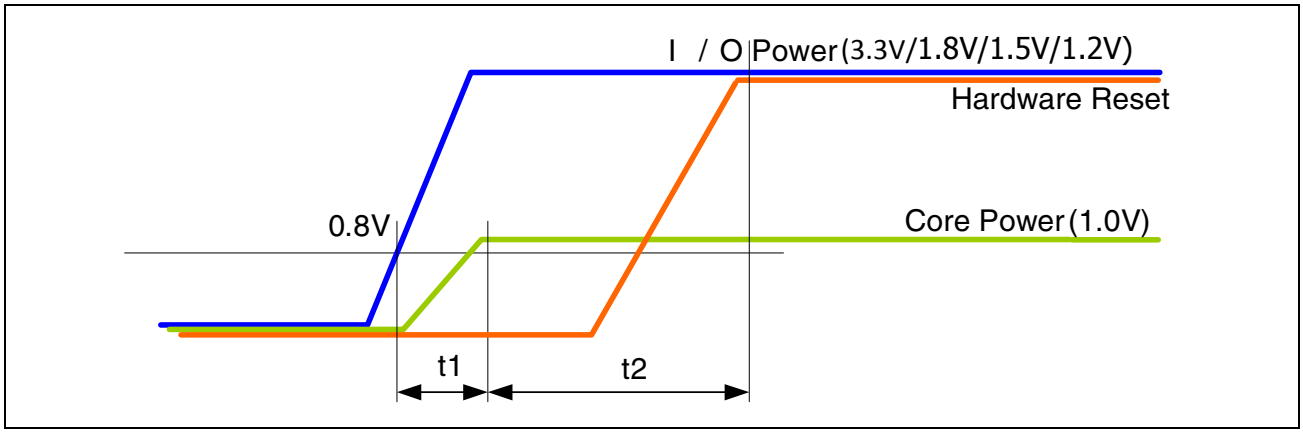
The initialization process loads all the pin-configurable modes (such as BSC slave address bits), clears all switching tables that are automatically maintained by the device, and places the switch in a disabled and idle state. Using the active PCIe bus, further initialization must be performed to configure the ports, MACs, and the tables before switching of packets can occur.

Power Sequencing

As in any multi-supply system, during the power ramp-up period, the I/O pads are in an undetermined state, and bus contention and current spikes could result. This can be minimized by an orderly and rapid power ramp up sequencing:

- The I/O power (3.3V/1.8V/1.5V/1.2V) should come up first, followed by the core power (1.0V). This implies that the core power (1.0V) should not be ON until the I/O power (3.3V/1.8V/1.5V/1.2V) reaches at least 1.0V.
- When the core power reaches the nominal core voltage (1.0V ±5%), the I/O power should be stable at the nominal I/O voltage (3.3V ±5%, 1.8V ±5%, 1.5V ±5%, 1.2V ±5%).
- The maximum ramp-up time for the core power 1.0V (from 0V to nominal voltage ±5%) is t1 = 5 ms as shown in Figure 4. Additionally, for a successful power-up sequence, Broadcom recommends that the external hardware reset should stay active for at least t2 = 40 ms after both the I/O and core powers are stable (see Figure 4).
- The VDDC (1.0V core) must be powered up at the same time or before the GP_AVDDL (1.0V analog) supply.

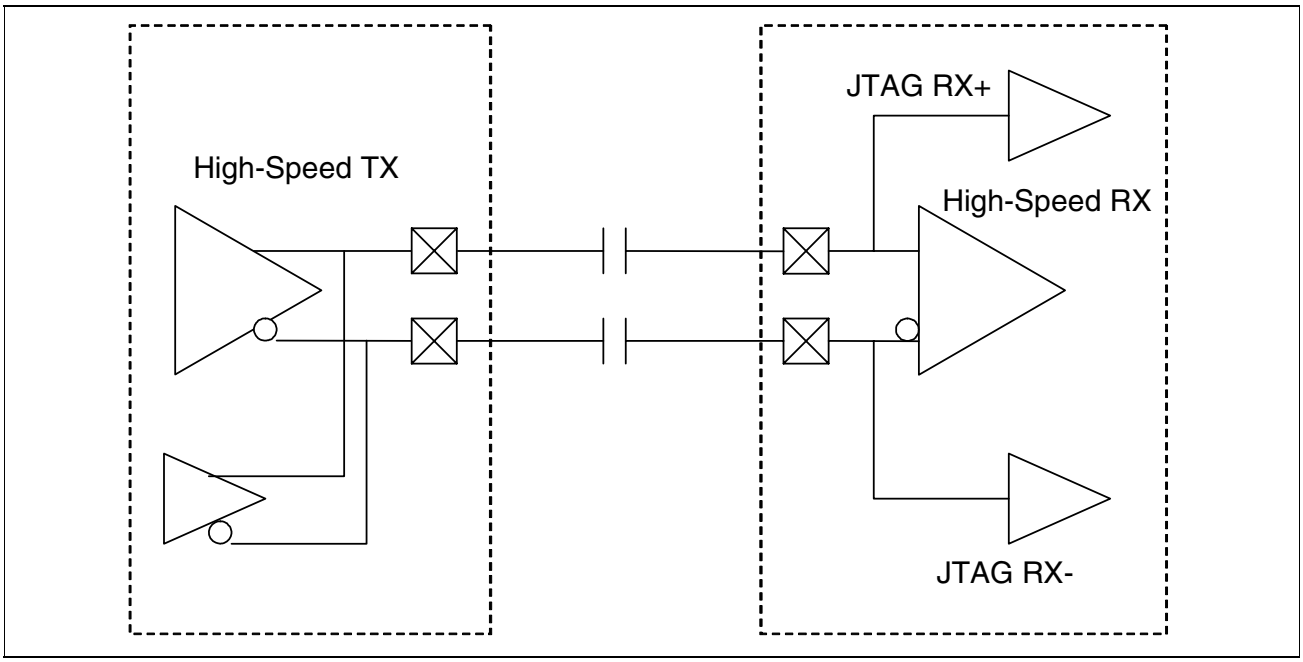
Figure 4: Power Sequencing



JTAG

Traditional JTAG provides the capability to test for opens and shorts conditions when the device is mounted onto the PCB, based on a direct connection. Present technology, where most high-speed differential signals are required to be AC-coupled, can produce false results due to traditional DC tests for opens and shorts. To provide a means of testing high-speed differential signals, the BCM56150 supports the latest JTAG specification IEEE Std.1149.6 (also known as AC-JTAG). To determine manufacturing faults on a high-speed differential line within a PCB, the device incorporates independent transceivers with low-load capacitance to avoid any adverse effect on the high-speed differential line (see Figure 5).

Figure 5: AC-JTAG Test Block



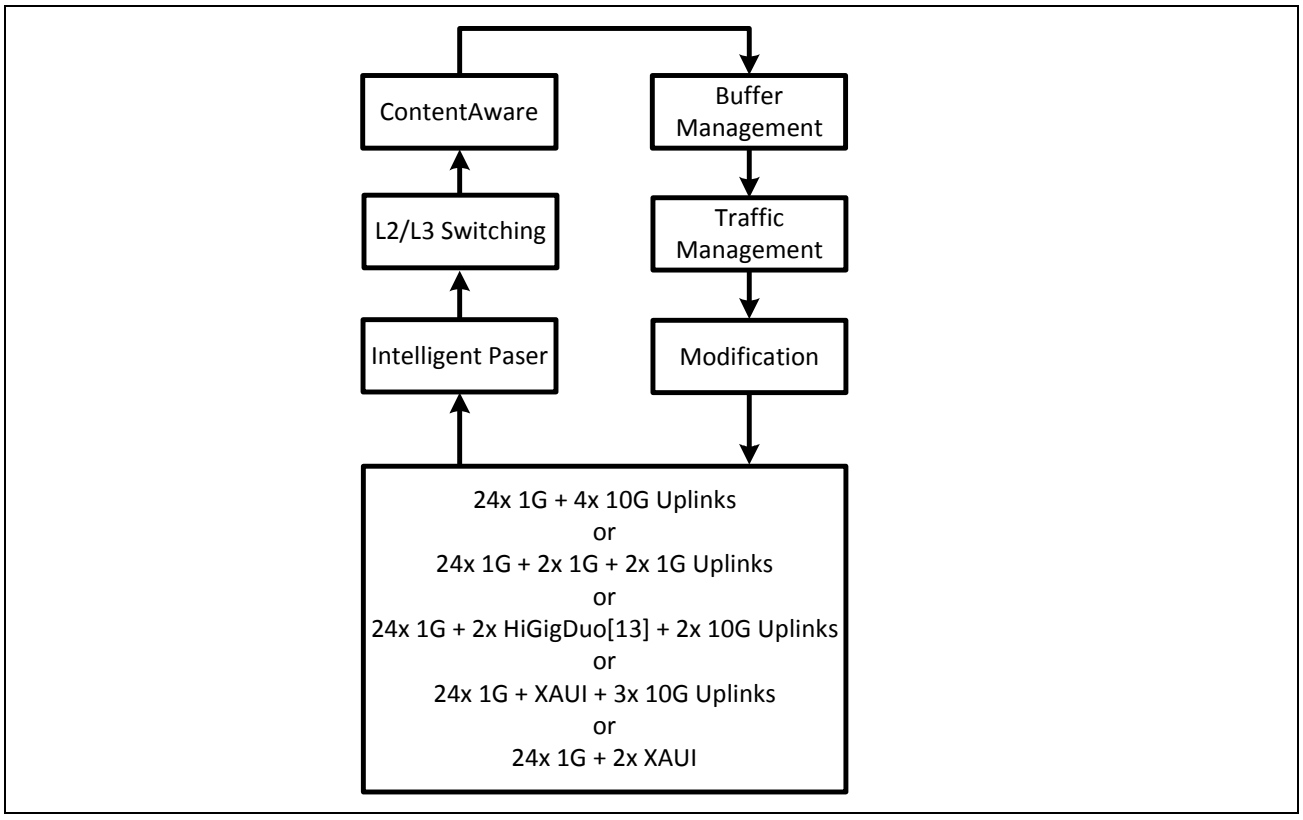
Section 3: Ethernet Switch Controller Features Description

Architecture

The integrated Ethernet Switch Controller has a modular, high-performance pipelined packet-switching (BroadScale™) architecture. This enables:

- Cost reduction
- Migration to different process technologies without architectural changes
- Flexible port configurations
- Scalable throughput
- Scalable custom features

Figure 6: Typical BCM56150 BroadScale Switching Architecture



Feature Overview

Some switch features and port counts may vary depending on the device ID (see “Overview” on page 19 for additional details).

Table 2: Switch Features

Feature	*Description*
Configuration	• Versatile port configurations. See Table : “,” on page 19 for overall configuration and Flexible SerDes Warpcore contains four SerDes lanes: – Supports 10GbE across a single lane: XFI/SFI – Supports 1GbE across a single lane • Dynamic buffer management • Supports: – Ethernet/IEEE 802.3 packet sizes (64 bytes to 1522 bytes). – Jumbo packets up to 9216 bytes.
L2 Switching	• Supports: – Learning up to 16K MAC addresses depending on device. – Static entries. – MAC limiting per port/LAG/VLAN. • Line rate switching for all packet sizes. • Shared and Independent VLAN learning. • VLAN flooding for broadcast and DLF packets. • Hardware-based address learning. • Six CPU-Managed Learning (CML) modes per port. • Hardware-and software-based aging. • Software insertion/deletion/lookups of the L2 table. • Same port bridging supported.
L2 Multicast	• Supports 1K L2 multicast groups. • Line rate switching for all packet sizes. • Three port filtering modes to control multicast packet behavior.
VLAN	• Supports 4K VLANs and assign VLAN for untagged and priority tagged packet on: – MAC-based VLANs – Protocol-based VLANs – IP-subnet based VLANs – Flow based VLAN – IEEE 802.1p – IEEE 802.1Q • Port-based VLAN • Independent and Shared VLAN Learning (IVL). • Ingress filtering for IEEE 802.1Q VLAN security. • VLAN-based packet filtering. • VLAN translation on ingress and egress.

Table 2: Switch Features (Cont.)

Feature	*Description*
VLAN Double Tagging	• Support for IEEE 802.1ad provider bridging: – Unqualified learning/forwarding. – Ability to add, remove, and translate (replace) both service-provider VLAN tag and customer VLAN tag. – Support for four programmable outer TPIDs with non-overlapping VLANs. • Support for double tagging requirements of Broadband Forum TR-101 – Packet forwarding is supported based on: • S-VLAN bridging (L2 switch based on MAC_DA and S-VID). • S-VLAN cross-connect: Destination port is based on S-VID only. • Double VLAN cross-connect: Destination port is based on (S-VID, C-VID) combination. – Supports for 2K shared {S-VID, C-VID}.
VLAN Range Based Double Tagging	• Allows a range of CVIDs to be mapped into the same SPVID without consuming multiple entries in the VLAN translation table. • Supports 128 VLAN range profiles. • Each VLAN range profile have a set of eight VLAN ranges configurable by software.
Source Port Filtering	• Egress port block masks. • Trunk group blocking masks.
Storm Control	• 4 meters for packet-based or byte-based rate control with the below packet types: – Unknown unicast (DLF) packet rate control. – Broadcast packet rate control. – Known L2MC packets rate control. – Unknown L2MC packets rate control. – Known IPMC packets rate control. – Unknown IPMC packets rate control. – Enable individual threshold per port.
Spanning Tree	• Supports: – IEEE 802.1D spanning tree protocol (single spanning tree per port). – IEEE 802.1s for multiple spanning trees. – IEEE 802.1w rapid spanning tree protocol—delete and/or replace per Port, per VLAN, or per Port per VLAN. • Spanning tree protocol packets detected and sent to the CPU.
802.3ad Link Aggregation	• 128 trunk groups supported with up to eight members per group. • No adjacency limitation. • Traffic load distribution for L2 switched and L3 routed packets. • Trunk port selection based on hash on source/destination MAC, VLAN, EtherType, source/destination IP address, TCP/UDP ports. • Trunk port selection for DLF, broadcast, and multicast packets.

Table 2: Switch Features (Cont.)

Feature	*Description*
Mirroring	• Ingress/egress mirroring support. • Mirror-to-port receives unmodified packet for ingress mirroring. • Mirror-to-port receives modified packet for egress mirroring. • Mirroring across stacked modules. • Remote Switched Port Analyzer (RSPAN) mirroring, VLAN mirroring, flow mirroring. • Encapsulated Remote Switched Port Analyzer (ERSPAN) mirroring. • Mirror-to-port can be a link aggregation group.
DSCP	• Per port DSCP remarking. • DSCP remarking based on a FP filter match. • DSCP to 802.1p mapping. • Remap incoming DSCP to new outgoing DSCP.
L3 Routing (IPv4, IPv6)	• 1024 (IPv4) or 512 (IPv6) hosts line rate routing for all packet sizes and conditions. • Supports: – Directly-attached hosts in the L3 table. – Longest prefix match (LPM) based routing. • Software based aging support. • Up to 512 LPM entries (IPv4) or 512 LPM entries (IPv6).
IP Multicast	• Line rate operation for all packet sizes and conditions. • Simultaneous L2 bridging and L3 routing. • Flexible multicast packet replication support for up to 4K VLANs. • Optional source port and VLAN checks. • Dual lookup: {S, G, V} and {*,G, V}. • PIM-SM, PIM-DM, PIM-SSM, and DVMRP on a per VLAN basis. • Reverse path forwarding checks. • Ability to fall back to L2 multicast lookup on IPMC miss. • Port Filter Mode (PFM) per VLAN for L2 multicast, IPv4 multicast, and IPv6 multicast packets. • Control trapping of unknown IPMC packets to CPU on a per VLAN per IP-type basis. • IP multicast address consistency check with destination MAC address.

Table 2: Switch Features (Cont.)

Feature	*Description*
ContentAware - Ingress Filter Processing	• Up to 2K FP rules with 8 slices allowing 8 parallel lookup and match. • Layer 2–7 packet classification. • Intelligent Protocol Aware processor with backward compatible byte-based classification option. • Parses up to 128 bytes per packet . • Multiple look-ups per packet. • Supports: – Multiple matches and actions per packet. – ACL-based policing. – Ingress/egress port based filtering. – MAC destination address remarking. – Class-based marking for SLAs. – Traffic class definition based on the filter. – Classification of different packet formats (IPv6, IPv4, double tagged, HTLS, IEEE 802.1Q, Ether II, IEEE 802.3). • Hierarchical min/max programmable meters allows policing of flows. • Metering granularity from 8 Kbps to 1 Gbps. • Dual leaky bucket meters support two rate three-color marking. • srTCM, trTCM, and modified trTCM (RFC2697, RFC2698, and RFC4115). • Metering support on ingress ports and CPU queues. • Jumbo packet metering. • TCP/UDP port number range checking. • IPv6 filtering (128 bits). • Filtering IP packets with options.
ContentAware -VLAN Filter Processing (VFP)	• Up to 512 FP rules with 4 slices. • Flexible VLAN assignment for untagged and tagged packets based on L2-L4 fields. • Q-in-Q featurability includes modifications to fields within inner or outer tags. • Field selectors on per port, per slice, and per packet type basis. • Ability to add or replace VLAN tag(s), change priority, assign classification ID, or drop.
ContentAware - Egress Filter Processing (EFP)	• Up to 512 FP rules with 4 slices. • Filter on fully modified packets allowing egress ACLs. • Filter on modified L3 routed and IPMC replicated packets. • Keys based on L2-L4 fields for IPv4 and IPv6 packets. • Actions: drop, change DSCP, change inner/outer priority, change inner/outer VLAN ID, change outer, and TPID. • Byte-based and packet-based statistics. • Egress metering (policing): Flow mode, srTCM, trTCM, modified trTCM.

Table 2: Switch Features (Cont.)

Feature	*Description*
QoS Features	• Eight CoS queues per port. • Enhanced 8 CoS queues for CPU. • Three drop precedence colors. • Per port, per CoS drop profiles. • Minimum/maximum bandwidth guarantee (shaping) per CoS, per port. • Traffic shaping available on CPU queues: bandwidth based and packet-per-second based. • Programmable priority to CoS queue mapping. • Provides two levels of drop precedence per queue. • Strict Priority (SP), Weighted Round Robin (WRR), and Deficit Round Robin (DRR) mechanism for shaped queue selection. • Simple Random Early Detection (RED) active queue management. • Programmable bucket size of egress port shaping and COS shaping. • Support for ingress port rate based policing and pause flow control. • Mapping of incoming priority, CFI to outgoing priority and drop precedence.
Port Security	• Supports 802.1x. • Blocking of egress ports on per ingress port or LAG basis (source port filtering). • Blocking of egress ports on per MAC address basis. • Blocking of egress ports for broadcast, unknown unicast, and multicast packets.
Denial of Service (DoS) Attack Prevention/Protocol Checkers	• Built-in illegal address check (IPv4, IPv6). • Denial of Service detection/prevention. • Land packets (SIP = DIP). • NullScan (TCP sequence number = 0, control bits = 0). • Ping flood (flood of IPMC packets). • SYN/SYN-ACK flooding. • SYN with sPort < 1024. • Smurf attack. • Individual control over handling of DOS packet.
CPU Protocol Packet Processing	• Ability to individually control CPU protocol packet handling, including BPDU, Address Resolution Protocol (ARP), Internet Group Management Protocol (IGMP), Multicast Listener Discovery (MLD), and DHCP. • Individual control of trapping protocol packets and setting internal priority. • Extensive control of handling of IGMP and MLD packet types.

Table 2: Switch Features (Cont.)

Feature	*Description*
Stacking Links	• Supports L2/L3 across stacked modules • L2MC • VLAN membership supported across stacked modules • Seamless CoS support • Mirroring and remote mirroring support • Supports up to 64 stacked modules • IPMC • Trunking of stacking ports • ContentAware processing on stacking port
Management Information Base	• sFLOW support, RFC3176. • RMON statistics group, IETF RFC2819. • SNMP interface group, IETF RFC1213, 2836. • Ethernet-like MIB, IETF RFC1643. • Ethernet MIB, IEEE 802.3u. • Bridge MIB, IETF RFC1493.
Energy Efficient Ethernet™ (EEE)	• System power saving by informing GPHYs into Low Power Idle (LPI) state. • EEE is only supported on 1GbE ports, not on the TSC uplink/stacking ports.

Memory

The BCM56150 device integrates all table memory necessary to support its functions. Table 3 indicates the major internal table memory allocations and their functions for switching, routing, and classification.

Table 3: Switch Internal Memory Table

Table Name	*Size*	*Function*
Port Table	One entry per each GbE, and CPU port	Per port configuration settings and attributes, i.e., L2 learning, port discards, VLAN handling, priority assignment.
IP Subnet-Based VLAN Table	256 Subnets	Assigns VLAN based on source IP subnet for untagged and priority tagged packets.
MAC-Based VLAN Table	2K MAC addresses	Assigns VLAN based on source MAC address for untagged and priority tagged packets. This table is shared with the VLAN Translation table.
IPV4-MAC Binding and ARP Spoofing Table	2K table for ingress[a]	Checks the IPV4-MAC binding of IP packets as well as ARP/ RARP request/reply messages for sender IPV4-sender MAC address binding.
VLAN Translation Table	2K table for ingress 2K table for egress	Translates VLAN between customer VLAN and service provider VLAN for provider bridging. This table is shared with MAC-based VLAN table.
Protocol-Based VLAN Table	16 per port	Assigns VLAN based on packet protocol for untagged and priority tagged packets.
VLAN Table	4K VLANs	Indicates port membership and spanning tree group for each VLAN.
DSCP Table	1920 entries	Remaps ingress and egress DSCP to new DSCP and priority.
Spanning Tree Group Table	256 groups	Indicates spanning tree state for each port for each spanning tree group.
MAC Address Table	16K MAC addresses	Contains learned and programmed MAC addresses: indicates destination port and additional properties of each MAC address, i.e., source/destination discard, priority, blocking, mirroring.
Reserved MAC Address Table	128 entries	Contains reserved MAC addresses, programmed by software for special handling, i.e., copy to CPU, drop, flood, for control packets, BPDUs. Reserved MAC Address table can also be used as an overflow for MAC address table. The only difference between these two tables is that the Reserved MAC table is managed by software.
MAC Block Table	32 groups	Allows for selective blocking and flooding to egress ports based on source MAC address groups.
Layer 2 Multicast Table	1024 groups	Indicates port membership for Layer 2 multicast groups.
Link Aggregation Group Table	128 groups	Indicates port membership of link aggregation groups and hash selection criteria.

Table 3: Switch Internal Memory Table (Cont.)

Table Name	Size	Function
Layer 3 Host Route Table	1024 IPv4 hosts 512 IPv6 hosts	Contains host IPv4 and IPv6 addresses for Layer 3 host routing, used as ARP cache.
Layer 3 LPM Route Table	512 IPv4 routes 512 IPv6 routes	Contains IPv4 and IPv6 subnets for longest prefix match routing, including ECMP/WCMP routing.
Layer 3 IP Multicast Table	256 groups	Indicates port membership for Layer 3 IP multicast (S,G) or (*,G) lookups, and controls replication of IPMC packets on egress ports with multiple VLANs.
Ingress ContentAware Processor Table	2K rules, 8 parallel lookups	Rules for L2–L7 packet classification on ingress, ACLs, metering, statistics

a. Shared with Ingress VLAN Translation table.

Table 4: OAM Table

Table Name	Size	Function
LMEP	512	For generating hardware CCM packets.
LMEP DA	512	For generating hardware CCM packets.
L3 Entry IPV4 Unicast	1K	MP Group Lookup Table shared with IPV4 Unicast Route Entry Table.
MA Index	4K	Provide session id for each MEP and the opcode profile pointer.
MAID Reduction	512	Compare the reduced MAID from the packet to the configured value in the table.
MA State	512	Track the state of the local MEP for CCM packets.
RMEP	2K	Track the state of the remote MEP for CCM packets.
OAM Opcode Control Profile	16	For action control defined for processing each opcode.
OAM LM Counter	4K	Counters for OAM loss measurement.

Address Management

The BCM56150 switch contains all of the tables required to manage station MAC addresses on the device. The address table (also referred to as the L2 table) has space for 16K entries. New entries in the table are automatically learned when packets are received on the ports. These entries can also be updated or created by the CPU. Learning is based on the source MAC address and VLAN ID. Entries that are not used for an extended period of time are automatically aged out. The device can be configured to age static entries as well.

For any valid incoming packet, the source MAC address along with the VLAN ID (either from the packet or from VLAN tables inside the device) is used to search the tables. On a successful match of (S-MAC, VLAN-ID) the device performs station move checks. If the incoming port does not match a port in the MAC table, the entry is relearned with the new incoming port value.

The destination MAC address, along with the VLAN ID, is used as a search key for the packet's output port. If a match is found, then the packet is switched out on that port. If a match is not found, then a Destination Lookup Failure (DLF) occurs, and the packet is switched out on all ports that are members of the VLAN.

Class of Service

The IEEE 802.1D specification defines eight levels of priority 0–7, with priority 7 being the highest priority. This information is carried in the 3-bit priority field of the VLAN tag header. This service applies to all network ports.

The BCM56150 switch supports up to eight CoS queues per egress port. For tagged packets, the incoming packet priority can be mapped to one of the eight CoS queues, based on the priority field in the tag header or from the result of filtering mechanisms. For untagged packets, the CoS priority is derived either from a programmable field within the VLAN address tables or from the result of filtering mechanisms. After the packets are mapped into a CoS queue, they are forwarded or conditioned using either Strict Priority (SP), Deficit Round Robin (DRR), or Weighted Round Robin (WRR) schedulers.

Strict Priority-Based Scheduling

In SP policy, any packet residing in the higher priority queues is transmitted first. Only when these queues are empty, will packets in lower priority queues be transmitted. The disadvantage of this scheme is potential starvation of packets in lower-priority queues.

Weighted Round Robin Scheduling

In the WRR scheme, each queue is assigned a weight. The number of packets sent from each priority queue depends on the weight. Because the unit of the weight is one packet, the weight can be anywhere from 64 bytes to 1522 bytes, or 9216 bytes (when supporting jumbo frames).

> ***Example:*** If there are four CoS queues of A, B, C, and D and the respective weights are 4, 3, 2, and 1, and if the packets are present in all the queues, the packets are sent in the sequence of A1, B1, C1, D1; A2, B2, C2; A3, B3; A4, accordingly.

Deficit Round Robin Scheduling

The Deficit Round Robin (DRR) scheme provides relative bandwidth sharing across all active COS queues. The DRR weights are relative to each other. If minimum bandwidth is configured in this mode, then it is served first. Any excess bandwidth is then shared according to the DRR weights.

Simple Random Early Detection

The simple RED scheme works to proactively drop or mark frames before congestion becomes excessive. The goal is to detect the onset of persistent congestion and take action so that TCP sources contributing to the congestion back off gracefully, insuring good overall network utilization while minimizing frame loss.

Backpressure Handling

The BCM56150 switch supports mechanisms to handle backpressure, allowing for flexible flow control on packet transactions. The limit at which backpressure is detected is based on the amount of memory utilized by the packets on an input port. A backpressure message (XOFF) is sent when the lower of the two conditions (cell count limit or packet count limit) is reached. When the corresponding count goes below the high threshold and reaches the low threshold, an XON message is sent. This limit flow control is applied to the:

- IEEE 802.3x flow control. If the port is configured in full-duplex mode, IEEE 802.3x flow control is used and the MAC control PAUSE frame is sent to inhibit traffic on that port for a specified period of time.
- Enable jamming signal. If the port is configured in half-duplex mode and enabled to send a jamming signal, the jamming signal is asserted.

For ports that continue to receive packets, even after applying the above-noted flow control, the packets are discarded. Similarly, when the packets are switched out and the memory utilization falls below the limit, incoming packets are handled again. For full-duplex ports, another PAUSE frame is sent, with the time period set to 0, upon which the remote port can transmit again. For half-duplex ports, if the jamming signal was asserted, it will now be deasserted.

Per Port Packet Rate (Storm) Control

The BCM56150 provides a per port packet or byte rate control mechanism to prevent the packets from flooding into other parts of the network. These programmable threshold limits apply to all ports. Several types of packets can be monitored:

- DLF/Unknown unicast packets
- Broadcast packets
- Unknown L2 Multicast packets
- Known L2 Multicast packets
- Unknown IPMC Multicast packets
- Known IPMC Multicast packets

The packet types are flexibly mapped to four leaky bucket mechanisms, and packets are discarded if the respective bucket becomes out of profile.

Mirroring

Mirroring is a useful feature for monitoring the traffic coming in or going out on a particular port. A port can be ingress-mirrored or egress-mirrored. The mirrored-to port can be programmed as a sniffer port to monitor all traffic on the mirrored ports. When a port is ingress-mirrored, any packet received on that port is sent to a mirrored–to port, and any packet transmitted from the egress-mirrored port is also sent to the mirrored-to port.

The BCM56150 supports the following packet mirroring functions:

- Mirror frames destined for an egress-specific port (egress mirroring)

- Egress mirroring of packets sent by the CPU
- Mirror frames coming from ingress-specified port (ingress mirroring)
- Mirror frames coming from a specific ingress port sent to a specific egress port
- Mirror frames that match a certain rule in the filtering processor
- Mirror frames destined to a specific MAC address

The BCM56150 supports mirror across stack.

Spanning Tree Support

The BCM56150 provides a number of features for compliance with the IEEE 802.1D and IEEE 802.1S spanning tree support specifications, as well as some optimizations for IEEE 802.1W rapid spanning tree support:

- The state bits in the spanning tree group are configured by the CPU to indicate a specific spanning tree state, and the necessary action is taken on the incoming packet. The spanning tree states supported are: disable, blocking, listening, learning, and forwarding.
- Entries marked as static in the MAC table are not aged out.
- The MAC table entry allows for detecting a hit on an address entry. If there is no hit on an entry for the spanning tree age limit duration, the address entry is deleted.
- All non-reserved addresses are self–learned.
- Reserved addresses from 0x0180c2000000 to 0x0180c2000010 and from 0x0180c2000020 to 0x0180c200002F are detectable, and these packets are forwarded to the CPU.
- Supports multiple 256 spanning trees (IEEE 802.1s). Each VLAN can be associated with one spanning tree group, which allows spanning tree-per-VLAN operation.
- Support for IEEE 802.1W Rapid Spanning Tree Protocol, with the ability to delete MAC table entries or replace the associated port information based on search criteria such as port and VLAN.

IEEE 802.1D Support

The BCM56150 supports the IEEE 802.1D specification for traffic class expediting and dynamic multicast filtering support.

Port Filtering Mode A

Forwards all addresses. In this mode, forwarding operates as bridge filtering mode 1. The port bitmap from the VLAN tables is used to determine the destination ports.

Port Filtering Mode B

Forwards all unregistered addresses. In this mode, if the group MAC address registration entries exist in the multicast table, frames destined for the corresponding group MAC addresses are forwarded only on ports identified in the member port set, which is identified by the port bitmap. If the group MAC address does not exist in the multicast table, then Mode A filtering mechanism is used.

Port Filtering Mode C

Filters all unregistered addresses. In this mode, frames destined for group MAC addresses are forwarded only if such forwarding is explicitly permitted by a group address entry in the multicast table. In other words, if the group MAC address exists in the multicast table, then the packets are forwarded using the port bitmap from that entry. Otherwise, the packets are dropped.

IEEE 802.1Q Support

The BCM56150 supports the IEEE 802.1Q specification for virtual bridged local area networks by providing the following features:

- For untagged (frame without a VLAN header) or priority tagged (frame with a tag header of VLAN ID = 0) frames, the ability to assign a VLAN based on the Source MAC Address, Source IP Address, or on a protocol. If a match is not found via these tables, then a default VLAN ID can be assigned per ingress port.
- Identification of the GVRP address 0x01-80-C2-00-00-21 and forwarding these frames to the CPU.

Link Aggregation

Link aggregation or trunking is a mechanism which bundles together up to eight ports to form a port bundle or a trunk. The port bundle is like one logical link and is useful when high bandwidth and/or redundancy between switches are required. The features include:

- Trunk ports in a bundle are always configured for full duplex.
- Trunking of network ports provides aggregate throughput up to a maximum of eight front-panel ports per trunk group.
- Provides incremental bandwidth dependent upon requirements.
- Provides link redundancy. In case of trunk port failure, the trunk group is modified and the port that failed is removed from the group.
- Provides load distribution on the trunk ports.

The BCM56150 supports 128 trunk groups, and each trunk group can have up to eight trunk ports. The trunk links are selected using a hashing function based on a combination of: MAC DA, MAC SA, VLAN, EtherType, IP DA, and IP SA. The BCM56150 supports link aggregation, with no adjacency limitation, within the same switch module and across stack.

Note: The Uplink ports may be included as trunk link members.

Double-Tagging

The BCM56150 provides full support for double tagging as specified in the emerging IEEE standard, including the following features:

- The Service Provider VLAN ID (SPVID) can be inserted based on ingress port or ingress port and customer VLAN.
- The Protocol field on the SPVID is fully programmable.
- The priority bits in the SPVID can be programmed by the provider or from the customer VLAN tag in the packet.
- The ability to distinguish customer control packets (such as spanning tree BPDUs). They may be discarded or processed locally depending on configuration.

Forwarding Control Block Mask

On certain ports in the switch, DLF unicast and multicast packets should be prevented from being forwarded. However, broadcast packets should always be forwarded to all ports.

To implement this feature:

1. Three separate registers, UNKNOWN_UCAST_BLOCK_MASK, UNKNOWN_MCAST_BLOCK_MASK, and BCAST_BLOCK_MASK are bitmasks for unknown unicast, unknown multicast, and unknown broadcast packets.
   a. The bits not set in these bitmasks define a set of egress ports to which unknown unicast, multicast, and broadcast frames should be forwarded.
   b. To block broadcast packets to a specific port, the appropriate bit is set in the BCAST_BLOCK_MASK.
   c. To forward broadcast packets to all ports of the VLAN, set all the bits in BCAST_BLOCK_MASK to 0.
2. Ingress logic will pick up the port bitmap from the VLAN tables, using the VLAN ID assigned to the packet, for unknown unicast, unknown multicast, and broadcast packets.
   a. For unknown unicast packets, the port bitmap is ANDed with the UNKNOWN_UCAST_BLOCK_MASK bitmask.
   b. For unknown multicast packets, the port bitmap is ANDed with the UNKNOWN_MCAST_BLOCK_MASK bitmask.
   c. For broadcast packets, the port bitmap is ANDed with the BCAST_BLOCK_MASK bitmask.

ContentAware Processing

ContentAware processing is described in the following sections:

Ingress Filter Processor (IFP)

For packets ingressing on the GbE and 10GbE ports. Ingress lookups occur on L2 and L3 pre-routed packets. The IFP is a flexible and powerful ContentAware Filter Processor. Filtering can be done by parsing the first 128 bytes of the packet using either predefined protocol fields such as VLAN, L2, and L3 addresses or using User Defined fields. Assigning a new priority, route, drop, or redirecting the packet are some of the actions that can be performed.

Table 5: ContentAware Field Processor Sizes

	Slices	*Rules per Slice*	*Total # of Rules*	*Meters*	*Counters*	*Bits per Rule (Single Wide)*
IFP	8	–	2048	2048	2048	–

Ethernet Operation, Administration, and Maintenance

The BCM56150 supports the Ethernet Operation, Administration, and Maintenance (OAM) management capabilities within the Ethernet layer. The OAM support is divide in the following two areas:

- Link-Level OAM, IEEE 802.3ah, Clause 57
  - Link Monitoring: A mechanism to detect failed or degraded link status as well as the ability to poll any part of a peer's Management Information Base (MIB).
  - Fault Signaling: A mechanism to advertise detected path failures to peers.
  - Remote Loopback: A mechanism to support data link layer frame loopback for fault localization purposes.
- Service-Level OAM, IEEE 802.1ag and ITU Y.1731
  - Path discovery: A mechanism to determine the path taken by a destination MAC address, MIP by MIP, from one MEP to another MEP across an MA. Path discovery is performed with LinkTrace Messages (LTM) and LinkTrace Replies (LTR).
  - Fault Detection: A mechanism to detect connectivity failures as well as unintended connectivity between services. Fault detection is performed with Continuity Check Messages (CCM).
  - Fault Verification: A mechanism to diagnose and isolate faults within an MA. Fault verification and isolation are performed with LoopBack Messages (LBM) and LoopBack Replies (LBR).
  - Fault Notification: A mechanism utilized by a MEP to notify peer MEPs and MIPs of a CFM failure. Fault notification is performed with standard CFM messages.
  - Delay Measurement: A mechanism for measuring network delay and jitter characteristics to guarantee SLA.
  - Loss Measurement: A mechanism for measuring network loss characteristic to guarantee SLA.

Network Management Support

The BCM56150 provides a set of counters to support the following Management Information Base (MIB) specifications:

- RMON statistics group (IETF RFC2819)
- SNMP interface group (IETF RFC1213 and 2863)
- Ethernet-like MIB (IETF RFC1643)
- Ethernet MIB (IEEE 802.3u)
- Bridge MIB (IETF RFC1493)

CPU/Management Interface

In low-cost Layer 2 switching systems, the BSC interface can be used for the setup, configuration, maintenance, and management of the BCM56150-based switch system. In high-end systems, with CPUs running the sophisticated routing protocol stacks required to support multilayer switching functions, the PCIe Interface is necessary to fulfill the bandwidth and performance demands of real-time packet switching. It is also used to move data to and from the CPU or a PCIe uplink.

External CPU with PCIe Bus

The BCM56150 device has PCIe Interface that is conformed to the PCIe Version 2.0 specifications. The BCM56150 supports single lane of PCIe. No external glue logic is required to support this interface. The protocols and electrical requirements of the PCIe specifications are strictly implemented.

Energy Efficient Ethernet

The BCM56150 device support Energy Efficient Ethernet (EEE) to reduce power consumption by enabling the PHYs to enter a Low Power Idle (LPI) state, during extended idle periods that may exist between packets. The power savings aspects of EEE are largely implemented in the PHYs. However, the PHYs are reliant upon the MACs to inform them of when to enter and leave the LPI state. The MACs make these determinations by examining the state of the transmit queues associated with each MAC. The EEE signaling between a MAC and its PHY is conveyed by the SGMII signals between them. The EEE feature is only supported on 1GbE ports, not supported on the TSC uplink/stacking ports.

When the transmit MAC asserts its LPI signal to the PHY, the PHY transmits a sleep symbols on the wire for a short period. This informs the link partner's receive PHY that it is entering the LPI state. After the sleep symbols have been transmitted, a quiet period is entered where there is no signaling. At the beginning of the first quiet period, the receive PHY indicates to its MAC that it has entered the LPI mode. The transmit PHY interrupts the quiet period periodically to send refresh symbols that are used to keep PLLs, filters, and other functions in sync, so that the LPI state can be exited quickly. When the transmit MAC deasserts, the PHY wakes up and transmits wake symbols for a short period to the link partner's PHY, informing it that it is time to wake up. The time between the transmit MAC deasserting and its resumption of packet transmission may be adjusted upward from the minimum PHY wake up time to allow for other system components to wake up and be ready for packet reception. Therefore, an idle period may precede the appearance of the first packet after a LPI sequence.

In general, EEE operates in an asymmetric mode. Meaning, the transmit direction and receive direction may enter and exit the LPI state independently. For 1000BASE-T, however, symmetric operation is required in order to truly benefit from EEE. In symmetric mode, both the transmit and receive paths must be indicating with sleep symbols before either side will enter the quiet state. Therefore, the transmit half of a PHY will send sleep signals until either sleep symbols are received from the link partner or the PHY has been commanded to exit the LPI state by the MAC.

Section 4: Ethernet Switch Controller System Interfaces

Overview

The BCM56150 includes the following physical layer interfaces:

- GbE (QSGMII): Allows connection to 10/100/1000BASE-T physical layer devices
- MIIM (IEEE 802.3u): Communication with physical layer devices
- JTAG: For IEEE Std. 1149.6 boundary scan
- BSC: For low-speed configuration (as a slave) and low-speed communications (as a CPU-controlled master/slave)
- LED: For system LED support

Table 6: System Interfaces

Interface	*Description*
Uplink or stacking port	• TSC uplink port, full-duplex operation – Integrated up to 4 10G SerDes transceivers and associated PCS for native support of SGMII, XFI, XAUI™, 10GBASE-KR/CR/LR/SR interfaces. See Table on page 19 for details. – Support for Broadcom's proprietary HiGig+ and HiGig2™ header formats • Support for jumbo frames up to 9216 bytes
GbE (SerDes) port	• Up to 16 GbE ports, full-duplex mode of operation, compliant to IEEE 802.3 • Support for 10/100/1000 Mbps using auto-negotiation • Supports 2 QSGMII/SGMII interfaces • Support for jumbo frames up to 9216 bytes
CPU Interface	• Supports PCIe interface
Serial LED	• Control of up to 255 system LEDs at a 30 Hz refresh rate • Simple microcontroller with instructions optimized for LED control • Low-cost two-wire interface to system LEDs • 256 bytes of program RAM • 256 bytes of data RAM • Direct access to per port speed, duplex state, flow control state, link state, transmit and receive activity, and collision activity
Parallel LED	• 16 embedded ports • 3 parallel drivers
MIIM (MDC/MDIO)	• IEEE 802.3u-compliant MIIM interface for communication with external PHY devices • 2.5 MHz operation • IEEE 802.3 Clause 22-compliant • IEEE 802.3 Clause 45-compliant

Table 6: System Interfaces (Cont.)

Interface	*Description*
Broadcom Serial Control (BSC) bus	• BSC-compliant interface–The Broadcom serial control (BSC) bus is Philips® I^2C-compatible. • Supports slave mode, allowing an external microcontroller to configure the BCM56150 device • CPU-controlled master mode to communicate with other BSC devices
JTAG	• JTAG-compliant interface used to support boundary scan operations • 20 MHz operation

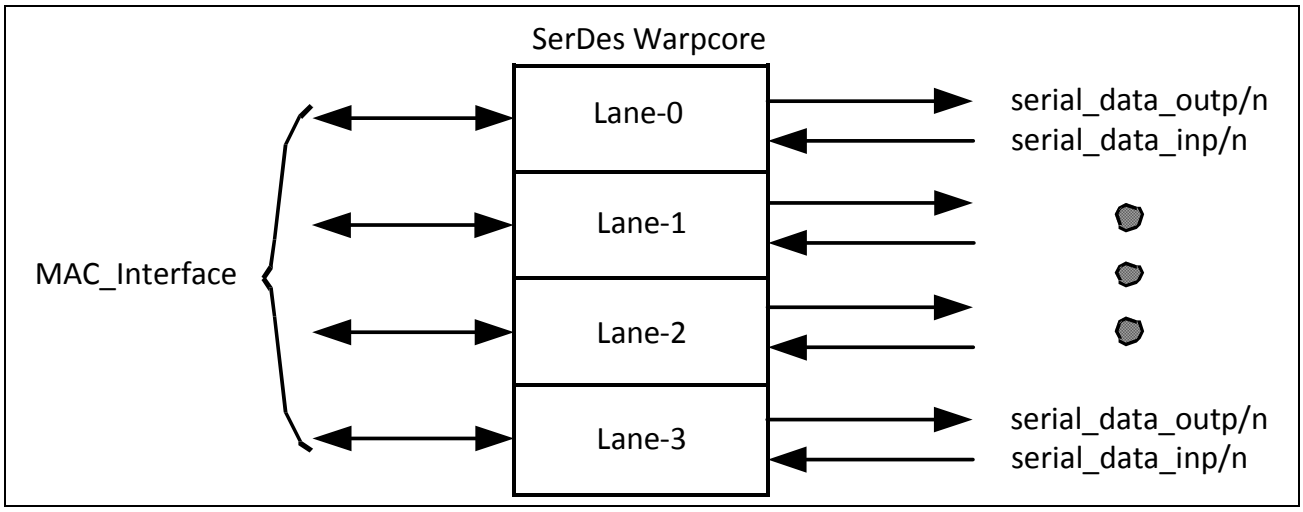
SerDes Warpcore

BCM56150 device family incorporates a macro called (TSC) TDM SerDes Warpcore. This macro allows the device to support low latency throughput, oversubscription capability and Flexport™ configuration. The TSC macro consists of the digital control logic and a Warpcore analog block. Throughout the document, TSC and Warpcore may be used interchangeably. A Warpcore is used at the physical interface, whereas a TSC is used at the application level.

The SerDes Warpcore is the versatile physical layer interface for the BCM56150. The device serial interface supports the following features:

- Support for line rates of 1.25 Gbps, 3.125 Gbps, 5.1625 Gbps, 6.5625 Gbps, 10.3125 Gbps, and 10.9375 Gbps per serial link.
- Quad SerDes block supporting four serial links.
  - Any port in a TSC can operate as 1G/10G mixed in a quad.
  - 1G/2.5G can also be mixed in a quad.
  - 2.5G/10G cannot be mixed in a quad.
  - 5.1625G cannot be mixed with any other speed mode in a quad.
- 5-tap DFE with adaptive control and VGA with AGC.
- Programmable RX equalizer with 0–8 dB boost, approximately 0.5 dB/step.
- Transmitter with 32-level post-cursor and 16 level precursor preemphasis. Figure 7 shows a conceptual block diagram.

Figure 7: Conceptual Block Diagram



HiGig+ and HiGig2 are supported across 1, 2, or 4 lanes. In 4 lane mode, the HG speeds supported are HG[10].

Note: When using HiGig or HiGig2 in the four–lane mode, the minimum IPG can be as low as 8 bytes.

Table 7 shows the TSC configurations.

Table 7: TSC Configurations

Lane Speed (Gbaud)	*# of Ports Supported*	*Encoding*	*Protocol: Interface*	*Ethernet Traffic (HiGig+)*	*Ethernet Traffic (HiGig2)*
1.25G	4	8b/10b	1GbE: 1000BASE-X, SGMII	N/A	N/A
3.125G	4	8b/10b	2.5GbE: 2500BASE-X	N/A	N/A
	1	8b/10b	10GbE: CX4, KR4, XAUI	N/A	N/A
	1	8b/10b	HG[10]: 4 x SerDes	10G	9.55G
5.1625G	4	64b/66b	5GbE	N/A	N/A
6.5625G	2	64/66b	HG[13]: 2 x SerDes	12.73G	12.15G
10.3125G	4	64/66b	10GbE: XFI, KR, SFI	10G	9.5454G
	4	64/66b	HG[10]: 1 x SerDes	10G	9.5454G
10.9375G	4	64/66b	HG[11]: 1 x SerDes	10.9375G	10.6061G

Note: A TSC can support either Ethernet or HiGig, but not both simultaneously. TSC can support any combination of Ethernet or HiGig/HiGig2 ports running at Ethernet rate. HG[10] with HiGig2 will result in lower than 10Gbps performance because the packet length is increased by 4 bytes.

TSC Ports

The BCM56150 includes two TSC for uplinks/stacking and/or cascade ports. These TSC ports can support 10-Gigabit IEEE 802.3ae Ethernet for both fiber and copper mediums. Each TSC can also be configured to support XAUI, two HiGig-Duo[13] ports or up to four 1G/2.5G/5G/10G ports. TSC does not support 100-FX, natively. If a TSC lane needs to support a 1000BASE-X/100-FX fiber port then an external PHY must be connected to support dual-speed optical fiber. The receive clock is recovered from the data stream. The HiGig-Duo[13] ports are used for connecting multiple BCM56150 devices together. The mode of the operation is configured by software. The HiGig port can operate in HiGig+™ or HiGig2 protocol. Figure 9.shows BCM56150 in cascade configuration. Figure 8 shows BCM56150 in non-cascade configuration.

Figure 8: BCM56150 in Cascade Configuration

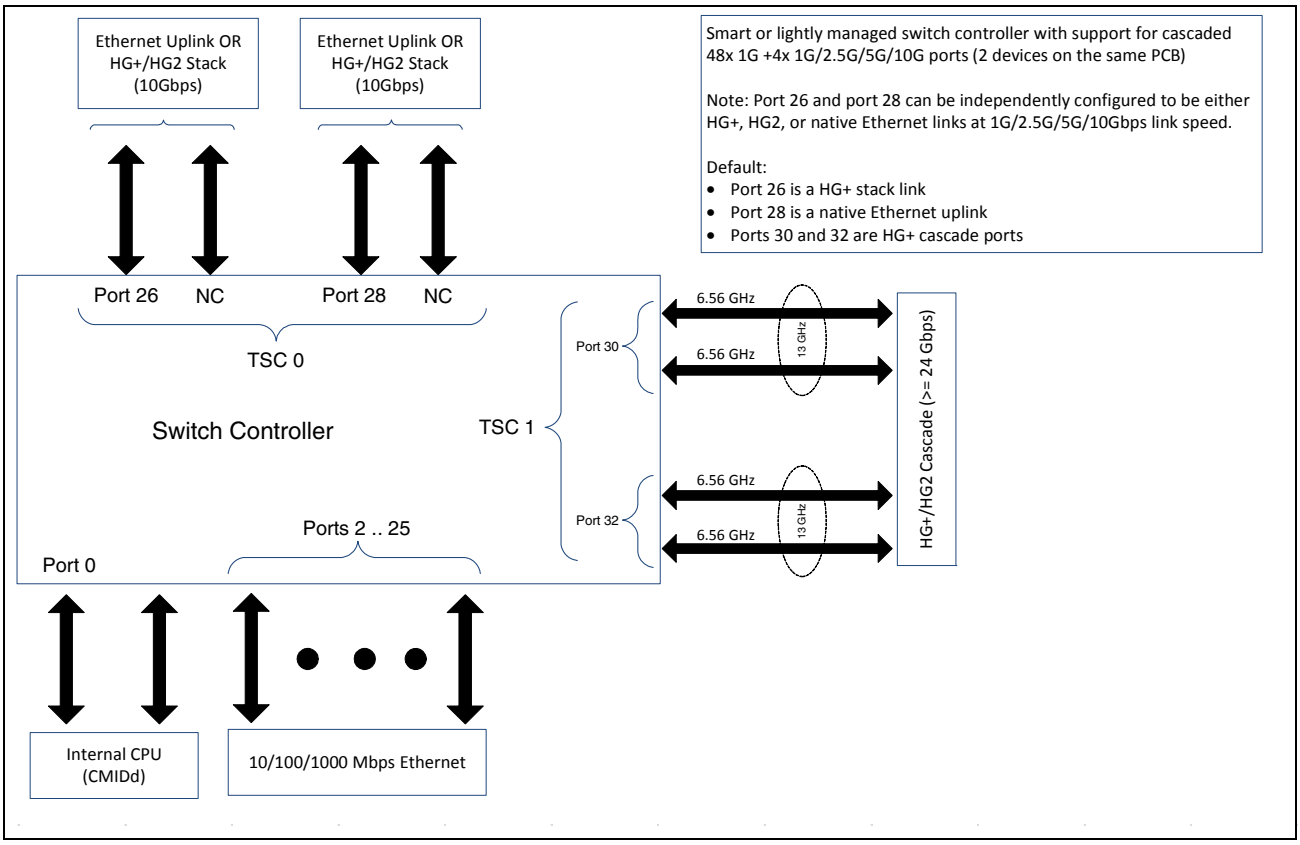
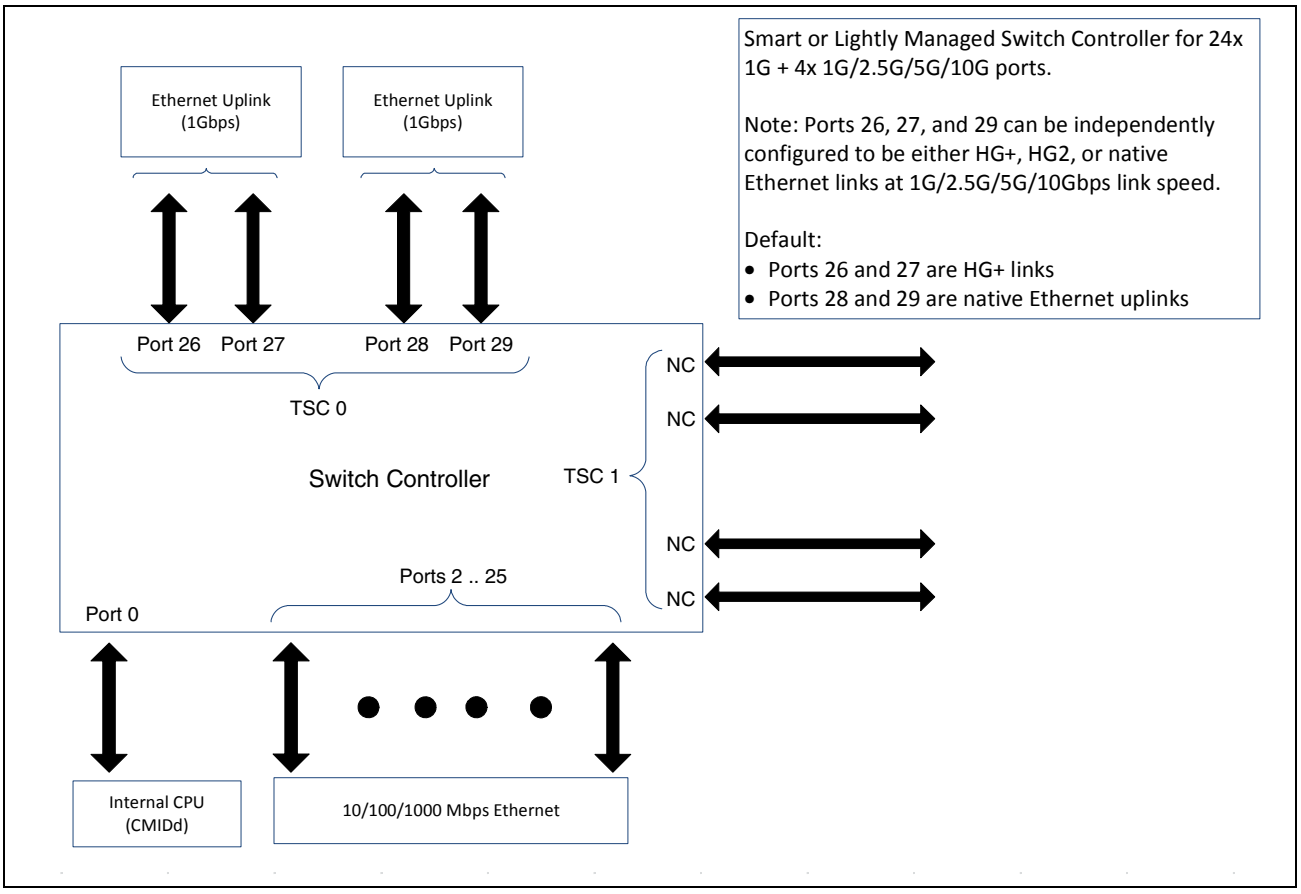


Figure 9: BCM56150 in Non-Cascade Configuration



The uplink/stacking port always connects to other uplink/stacking ports. The VLAN tag is not present in the Ethernet packet. Instead, the VLAN Tag Control field (VID, CFI, and PRIORITY) is part of the stacking packet header format. The 32-bit CRC is computed over the entire packet (including header and the Ethernet payload). The generation and verification of the CRC are done by the MAC transmit and receive logic, respectively.

10GbE (XAUI)

The BCM56150 supports 10-Gigabit IEEE 802.3ae Ethernet for both fiber and copper mediums.

The 10GbE port can be connected to XFP or XENPAK optical modules as shown in Figure 10 and Figure 11. This configuration supports link distances of up to 40 Km.

The 10GbE port also supports 10GBASE-CX4, based on twinaxial InfiniBand cable and connector as shown in Figure 12. This configuration supports link distances of up to 15 meters.

The interface is compliant with the XAUI interface specification for 10-Gigabit Ethernet, and it consists of four SerDes channels operating at 3.125 Gigabaud. Each channel receives and transmits data on a differential serial pair, resulting an effective data rate of 10 Gbps full-duplex.

Each 10GbE port can also support 2.5GbE and 1GbE on a per-port basis via auto-negotiation. In 2.5-GbE mode, only lane 0 of the 4 lane XAUI port is used to pass traffic at 2.5 Gbps (3.125 Gbps 8B/10B encoded speed SerDes interface). In 1 GbE mode, only lane 0 of the 4 lane XAUI port is used to pass traffic at 1 Gbps (1.25 Gbps 8B/10B encoded speed SerDes interface). Auto-negotiation on this interface is compliant with IEEE 802.3 Clause 37, extended via additional pages to support additional speeds, or through parallel detection.

The XAUI interface supports programmable transmit pre-emphasis and receive equalization.

The receive clock is recovered from the data stream.

Figure 10: XAUI Interface Connects the BCM56150 10GbE with the XFP Optical Module through BCM8704

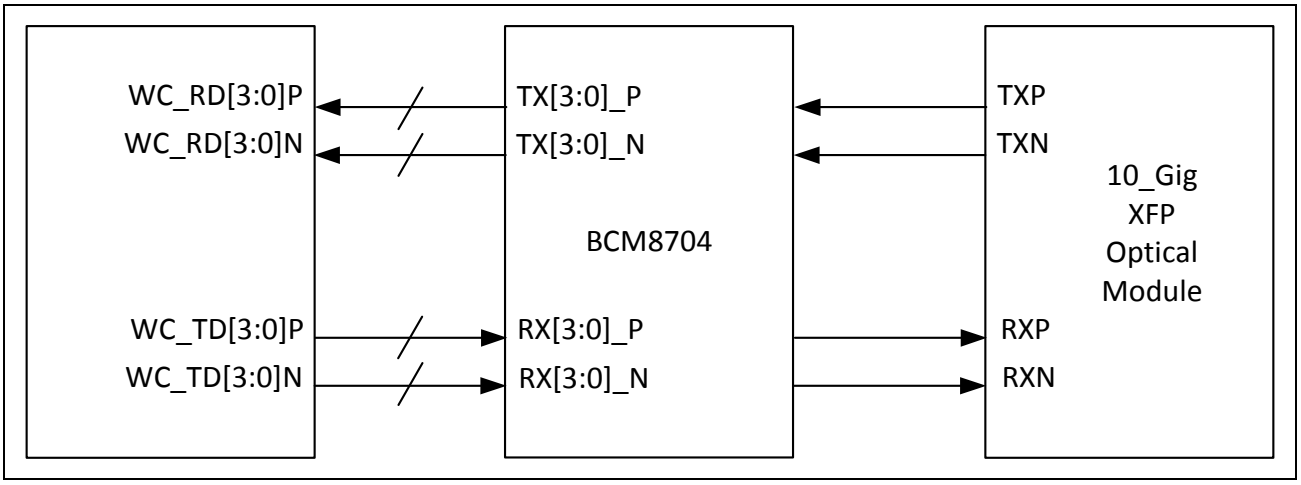


Figure 11: XAUI Interface Connects the BCM56150 10GbE with the XENPAK Optical Module

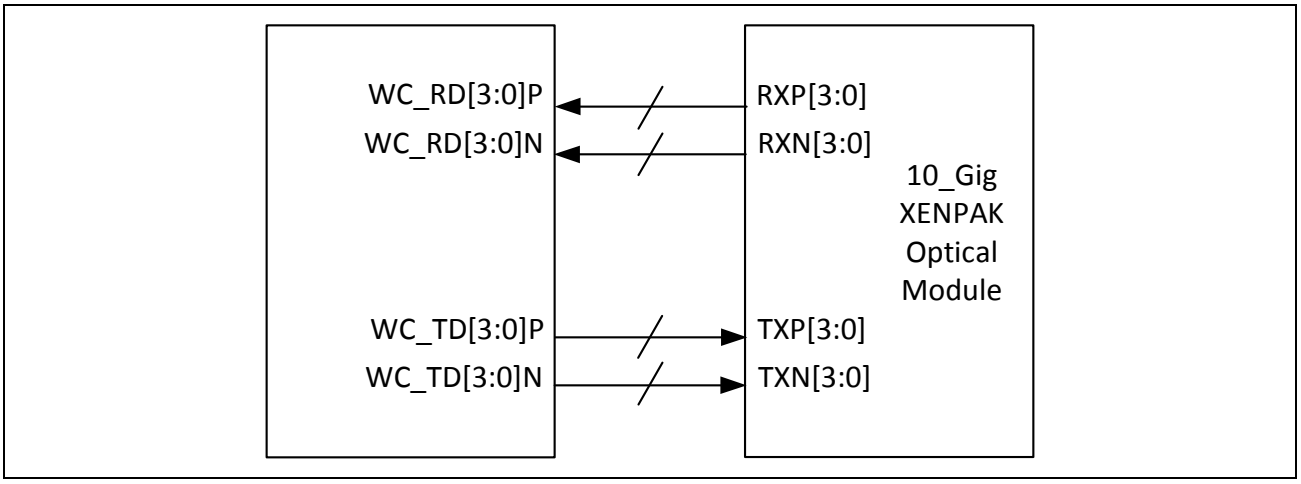
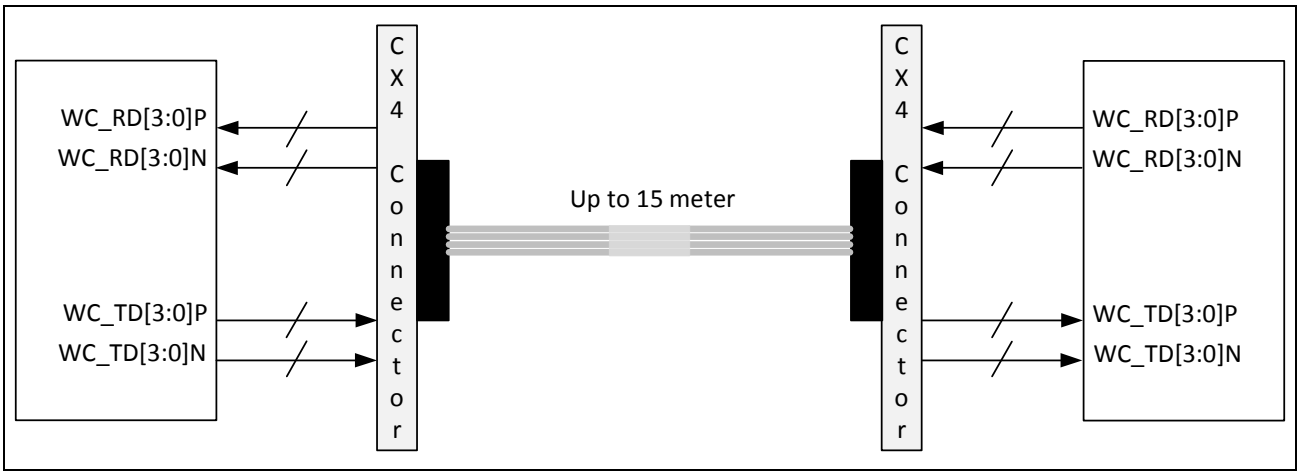


Figure 12: The BCM56150 10GbE Port Driving a Twinaxial InfiniBand Cable via the XAUI Interface



HIGIG+/HIGIG2 Interface

The HiGig+/HiGig2 interface complies also with the standard XAUI interface for 10GbE, but a proprietary Broadcom HiGig+/HiGig2 module header is added to each packet for interchip communication.

The HiGig+/HiGig2 protocol allows for many features across the stack link, including:

- VLAN transparency
- Port and traffic mirroring
- Trunking
- Daisy chaining of BCM561501 devices for multistage fabrics

HiGig_Lite Frame Structure

HiGig_Lite is a HiGig2™-like transmission protocol over the 1-GbE/2.5-GbE stacking ports. It keeps the existing GbE MAC unchanged by inserting 16 bytes of transmission protocol header between the preamble and the MACDA. The HGL is available for devices that have TSC ports operating at 1G/2.5G mode.

- The HG_Header is composed of two sections: the 8-byte Fabric Routing Control (FRC) header, and the 4-byte Packet Processing Descriptor (PPD) header.
- The HG_Payload carries Ethernet payloads starting from MACDA, excluding the CRC field.
- The HG_CRC performs the same function as the Ethernet CRC, but it covers HG_Payload as well as the HG_Header (FRC and PPD).

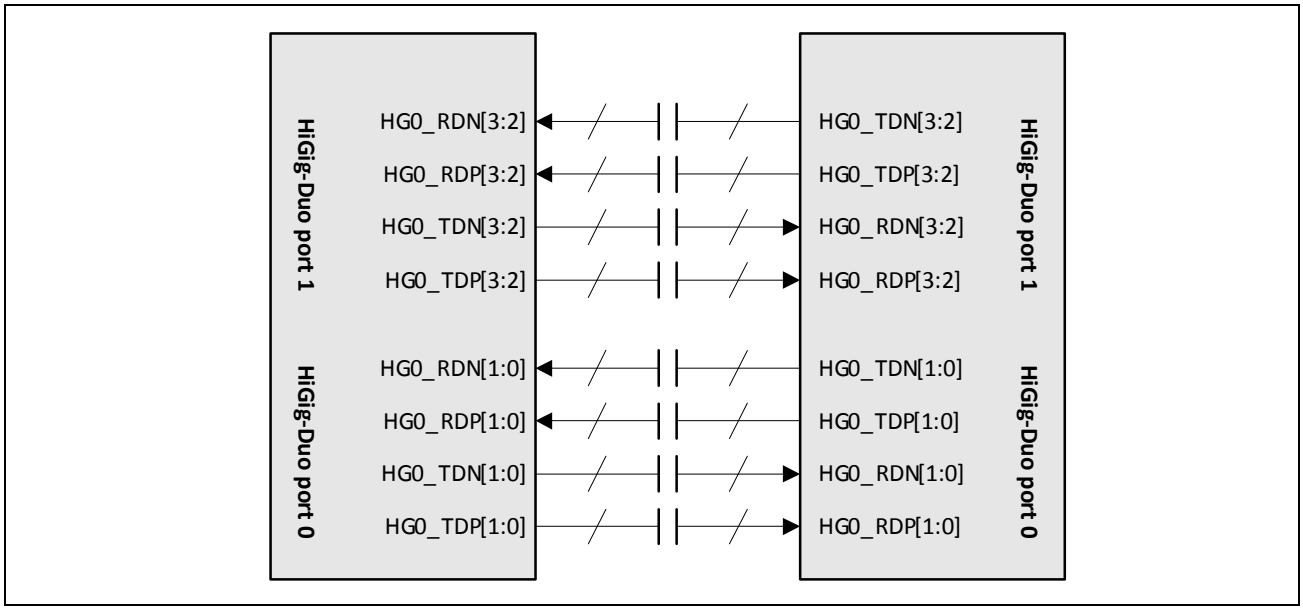
HiGig-Duo[13] Interface

The HiGig-Duo[13] mode can be configured by software. The HiGig-Duo interface uses channel consisted of two separate differential lanes to transmit and receive data. The receive clock is recovered from the data stream. Each channel is programmed to operate at 12.73 Gbps data rate (Table 8). These interfaces are used for connecting multiple BCM56150 devices. The connection of the HiGig-Duo[13] ports is shown in Figure 13.

Table 8: Data Rates of HiGig-Duo Ports

Port Configuration	*SerDes Frequency*	*Port Baud Rate*	*Port Data Rate*
HiGig-Duo[13]	6.5625G	13.125G	12.73G

Figure 13: HiGig-Duo Port Connection of 2 BCM56150



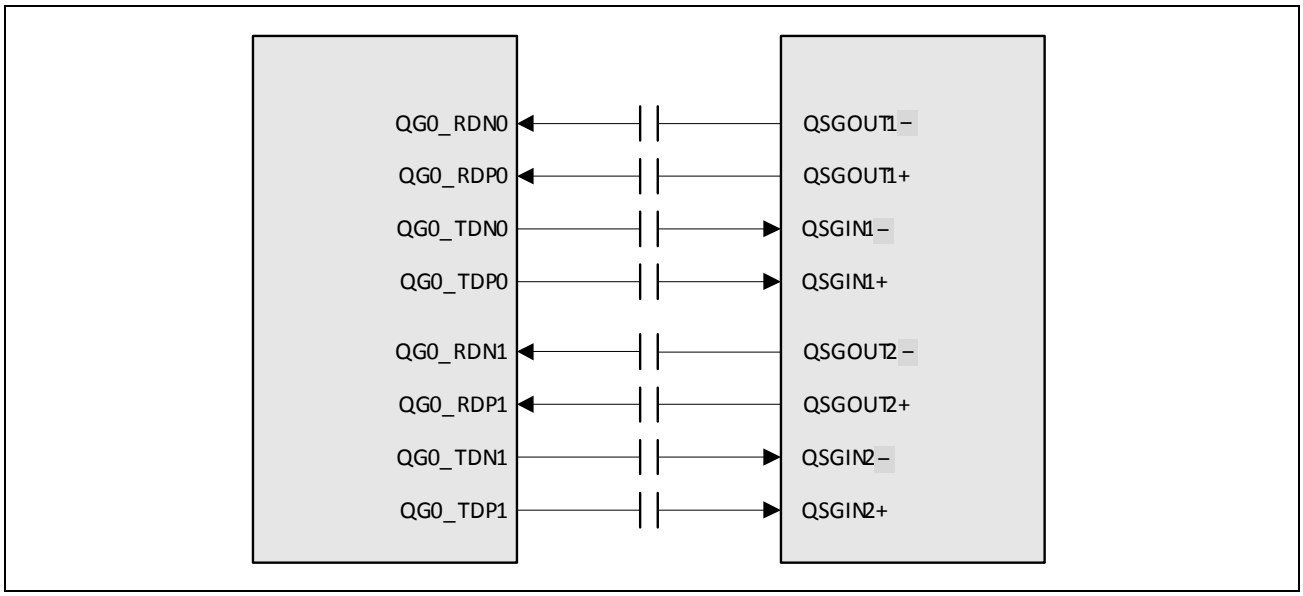
1G/2.5G/5G Interface

1G/2.5G/5G ports use a single lane to transmit and receive data. When set to 1GbE speed, the port supports SGMII (10/100/1000M) or 1000BASE-X (fiber) mode but does not support 100-FX mode. When set to 2.5 or 5GbE speed, the port can support 2.5 or 5GbE overclocked-Ethernet mode.

1GbE (QSGMII/SGMII)

The BCM56150 provides up to 2QSGMII links, each operating at 5.0 Gbps on two pairs of differential signals (1 TX pair and 1 RX pair). The QSGMII is a CML interface and connects to external QSGMII PHYs such as Broadcom's BCM54282. Each QSGMII link is an equivalent of four 1.25 Gbps SGMII links, conveying four ports of network data with significantly less number of signal pins compared to GMII or SGMII. With four GbE links multiplexed onto one QSGMII link, the data from port 0 will display first, followed by data from port 1, port 2, and port 3. This will then be followed by the next piece of data from port 0 and the rest of the ports following the same sequence. Since the data is 8b/10b encoded before being sent out the QSGMII link, the raw data throughput is 4 Gbps. The QSGMII operates in both half and full duplex and at all port speeds. The QSGMII link replicates the data 100 times and 10 times, respectively, when operating at 10 Mbps or 100 Mbps.

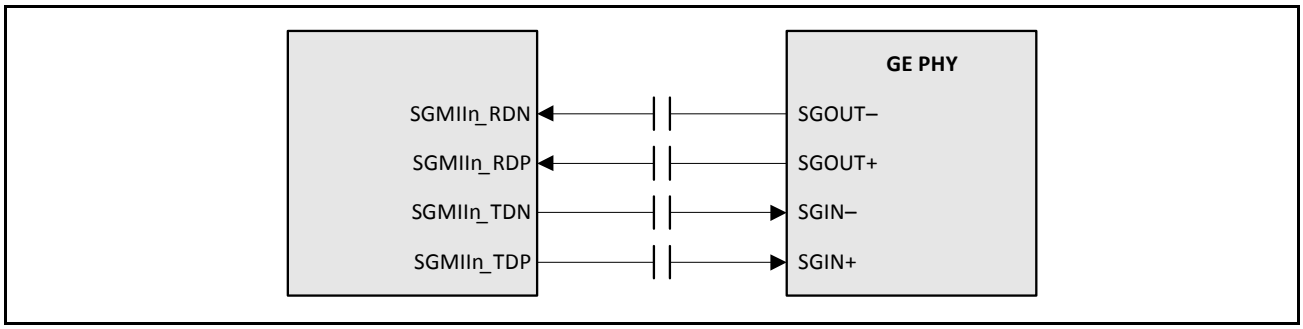
Figure 14: BCM56150 QSGMII Interface



The BCM56150 device can also configure the QSGMII interface into an SGMII interface. The transmit and receive differential pairs of each SGMII interface run at 1.25 Gbps. The receive and transmit clocks are embedded within the data stream. Because the data is 8b/10b encoded, the actual throughput is 1 Gbps. SGMII is a CML interface and commonly connected to an external PHY for a 10/100/1000BASE-T application. The BCM56150 supports auto-negotiation on its SGMII interface. When the device operates at 10 Mbps or 100 Mbps, the SGMII differential pair replicates the data 100 and 10 times, respectively.

The SGMII interface also can be configured in SerDes mode, which also operates at 1.25 Gbps. Again, with 8b/10b encoding, the actual data throughput is 1 Gbps. Therefore, a typical application using this interface is fiber and can be connected directly to an optical module with an option of DC-coupled or AC-coupled for 1000BASE-X application.

Figure 15: BCM56150 SGMII Interface



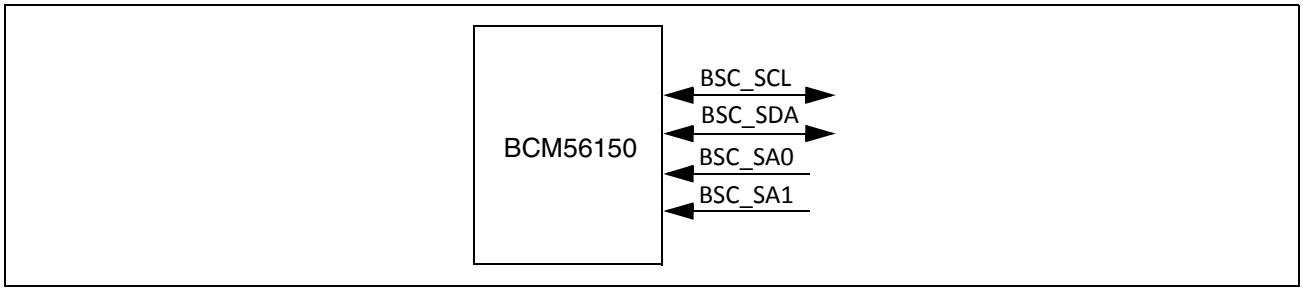
MII Management

The CPU Management Interface Controller (CMIC) supports an IEEE 802.3u standard MII Management (MIIM) interface. This is a two-wire serial bus controlled by the CMIC. It allows register access to all system PHYs. PHY data can be read/written–to using this interface. The two signals for MIIM are IP_MDC (clock) and IP_MDIO (bidirectional data). The CPU programs the PHY registers using this interface. After the initialization sequence, the CPU could read the link up/down register bit to detect any link changes. Alternatively, the CPU can enable the MIIM_AUTO_LINK_SCAN_EN bit. In this mode, CMIC will scans the PHYs and detect link status for each port. The link status register is updated at the end of each scan. If a link status change is detected, CMIC sends a notification to the CPU.

Broadcom Serial Interface (BSC)

The BCM56150 switch provides an BSC interface to communicate with other devices that support a similar interface. The signals supported are shown in Figure 16.

Figure 16: BSC Interface



The BSC interface can be configured to operate in either master or slave mode. The supported BSC data protocol format is big endian, which is consistent with the BSC protocol supported by other vendors.

Upon reset, the BCM56150 switch enters the default slave mode, provided BSC_MODE strap is pulled high. In this mode, an external BSC master device can communicate with the BCM56150 switch and initialize the device using the BSC_SDA and BSC_SCL lines. The external master can write the 16-bit address of the register to be accessed, followed by the 32-bit data to be written. When all 32 bits (4 bytes) of data are provided, a write to the internal register is performed.

Note: There is no mechanism to support any interrupt structure or bus mastering in the BSC slave-only mode.

A default BSC slave address of 0b1000100 is used for the slave-only mode. Additionally, the BSC_SA0 and BSC_SA1 inputs can be strapped high or low, to change the default slave address, giving a range of 0b1000100 to 0b1000111. Both 7-bit and 10-bit addressing schemes are supported.

Optionally, CPU-controlled master/slave mode is supported. This mode is disabled by default and is useful to connect other BSC devices, such as a time-of-day chip, temperature sensors, parallel ports, and so forth, to the BCM56150 switch. In master mode, read and write BSC operations are initiated under program control of the host CPU. A block of registers accessible by the CPU controls this function.

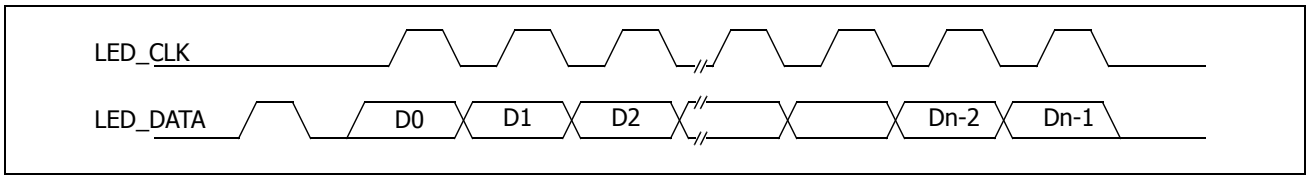
LED Interfaces

Serial LED Mode

A LED microprocessor controls the serial LED signals (clock and data). Both LED_CLK and LED_DATA are outputs. It can provide the port status for all GE and TSC ports. This requires programming some assembly code routines to run on the LED microprocessor. Please refer to the SDK and PRG for more details.

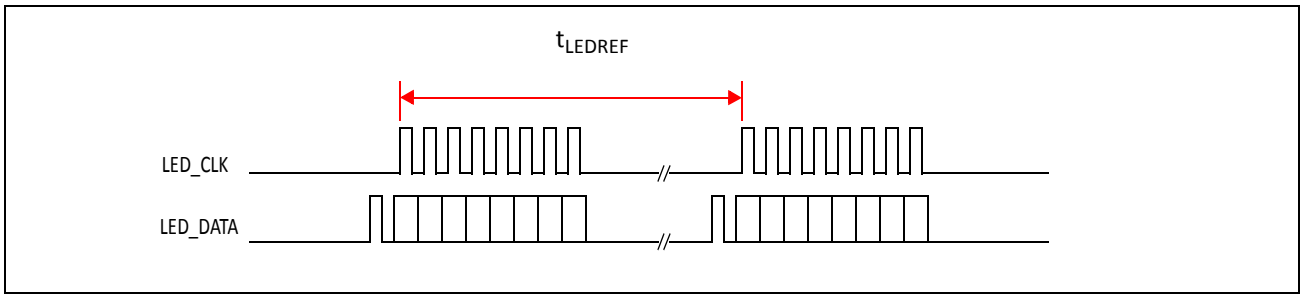
When active, LED_CLK is a 5 MHz clock. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED_DATA bits. The LED_DATA signal is pulsed high at the start of each LED refresh cycle (see Figure 17). The LED refresh cycle is repeated every 30 ms to refresh the LEDs.

Figure 17: Single LED Refresh Cycle



The LED refresh cycle is repeated periodically (every 30 ms) to refresh the LEDs (see Figure 18).

Figure 18: LED Refresh Cycle



PHY-driven Parallel LED Mode

In addition to the serial LED interface which provides status for all 24 ports, a 48-output parallel LED interface is available for the 16 integrated GPHYs. Parallel LED interface for the other 8 ports comes from the external QSGMII-based PHYs.

Note: Several LED pins behave as strap pins during reset and some LED pins are shared with the MII and GPIO interfaces. When either MII or GPIO interface is enabled then the LED function is disabled. Refer to Section 7: “Pin List Description,” on page 77 for more details.

The BCM56150 has three programmable LED balls per port that perform different functions. Each of the BCM56150 LEDs can be individually programmed to many available modes on a per port basis.

Serial to Parallel LED Mode

When the LED microprocessor is enabled, the parallel LED interface is also controlled by the LED microprocessor. It inputs the serial LED signals to the internal shift register circuit and outputs the LED signals on the parallel LED interface. In this mode, the LED signals come from the port status. It can support all GE and TSC ports, same as in serial LED mode. The LED signal count per port is controlled by the LED microprocessor code. It is not limited to three signals per port as in PHY-driven parallel LED mode. Since there are 48 pins in the parallel LED interface, it can output up to 48 LED signals.

Ethernet Time Synchronization (Synchronous Ethernet)

The BCM56150 supports Synchronous Ethernet Layer One Clock Recovery (ITU G.8261). The support includes two functions: controlling the transmit clock of the network ports and recovering a clock from a network port. The Synchronous Ethernet interface provides the primary (L1_RCVRD_CLK) and the backup recovered (L1_RCVRD_CLK_BKUP) clocks from any of the SerDes ports in the device to support L1 time synchronization. In addition to the clock signals, two valid signals are also provided to qualify the clock signals (L1_RCVRD_CLK_VALID and L1_RCVRD_CLK_VALID_BKUP). Both primary and backup recovered clock signals can be chosen from any of the ports in the device. The selection is done by register programming.

Note: The clock recovery is valid only for Warpcore and QGPHY ports.

Layer One Clock Recovery allows a clock to be recovered from the incoming data stream on any valid physical port. When implementing a synchronized Ethernet solution, a jitter attenuation PLL should be used prior to feeding the clock back to the reference clock input signals. A backup recovered clock is provided in addition to a primary recovered clock. Both clock sources provide an external signal indicating the validity of the clock. Since there is considerable delay in generating the external signal indicating the validity of the clock, an AND gate is used internal to the BCM56150 to gate off the clock from available Loss of Signal (LoS) pins.

IEEE 1588

Note: For high performance 1588 applications, it is recommended to run 1588 firmware stacks on the embedded CPU and SDK on the external host.

The BCM56150 is a highly integrated device with many hardware hooks for designs that require network time synchronization. The following features make the device ideally suited for time synchronization applications complying with IEEE 1588:

- Supported modes:
  - One-step E2E and P2P TC, two-step E2E and P2P TC
  - One-step BC, two-step BC (with clock recovery)
  - TC+OC Slave, BC+OC Slave (with clock recovery)
- One-step clock features:
  - On-the-fly egress packet modification including UDP checksum update and CRC update.
  - All modifications to Correction Field handled in hardware. Very short residence time.
  - All packets time stamped on ingress. Uses switch packet processing engines to identify 1588 packets.
- Two-step features:
  - Egress timestamps are stored in per port FIFO, along with 1588 Sequence number. CPU indicates which packets should generate a timestamp on egress.
  - All packets time stamped on ingress. Uses switch packet processing engines to identify 1588 packets and trap to CPU.
- Synchronizable timestamp counter:
  - Can be phase-locked to external source.
  - BroadSync™ (timecode + event clock) interface
  - Time stamped GPIOs
- Frequency Synthesizer:
  - Additional clock divider: 10 MHz + 1 pps

Section 5: Gigabit Ethernet Transceiver

Copper Interface

The BCM56150 can communicate with Link Partners that support 10BASE-T, 100BASE-TX or 1000BASE-T. The BCM56150 supports auto-negotiation for 10BASE-T, 100BASE-TX or 1000BASE-T. The BCM56150 supports force mode for 10BASE-T and 100BASE-TX. Force mode is not supported for 1000BASE-T operation.

The following sections describe the internal circuitry and additional features of the copper interface.

Encoder

In 10BASE-T mode, Manchester encoding is performed on the data stream that is transmitted on the twisted-pair cable. The multimode transmit digital-to-analog converter (DAC) performs pre-equalization for 100m of Category 3 cabling.

In 100BASE-TX mode, the BCM56150 transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first 2 nibbles of preamble with a start-of-stream delimiter (/J/ K codes) and appending an end-of-stream delimiter (/T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets. The encoded data stream is serialized and then scrambled by the stream cipher block, as described in “Stream Cipher” on page 61. The scrambled data is then encoded into MLT-3 signal levels.

In 1000BASE-T mode, the BCM56150 simultaneously transmits and receives a continuous data stream on all four pairs of the Category 5 cable. Byte-wide data from the transmit data signals are scrambled when the transmit enable is asserted, and the trellis (a PAM5 symbol on each of the four twisted-pairs) is encoded into a four-dimensional code group and then inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first 2-bytes of the preamble with a start-of-stream delimiter, and appending an end-of-stream delimiter to the end of the packet. When the transmit error input is asserted during a packet transmission, a transmit error code group is sent in place of the corresponding data code group. The transmitter sends idle code groups or carrier extend code groups between packets. Carrier extension is used by the switch to separate packets within a multiple-packet burst, and is indicated by asserting the transmit error signal and placing 0Fh on the transmit data signals while the transmit enable is low. A carrier extend error is indicated by replacing the transmit data input with 1Fh during carrier extension.

The encoding complies with IEEE 802.3ab and is fully compatible with previous versions of the Broadcom 1000BASE-T PHYs.

Decoder

In 10BASE-T mode, Manchester decoding is performed on the data stream.

In 100BASE-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT-3 to serial non-return to zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles, and the end-of-stream delimiter and idle codes are replaced with zeros. The decoded data is driven onto the MII receive data outputs. When an invalid code group is detected in the data stream, the BCM56150 asserts the MII receive error (RX_ER) signal. RX_ER is also asserted when the link fails or when the descrambler loses lock during packet reception.

In 1000BASE-T mode, the receive data stream is:

- Passed through the Viterbi decoder
- Descrambled
- Translated back into byte-wide data

The start-of-stream delimiter is replaced with preamble bytes, and the end-of-stream delimiter and idle codes are replaced with 0x00. Carrier extend codes are replaced with 0x0F or 0x1F. The decoded data is driven onto the QSGMII receive data outputs. Decoding complies with IEEE 802.3ab and is fully compatible with previous versions of Broadcom 1000BASE-T PHYs.

Link Monitor

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the following pairs for the presence of valid link pulses.

- TDP_[73:0]_[0]/TDN_[73:0]_[0]
- TDP_[73:0]_[1]/TDN_[73:0]_[1]

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal is detected on the receive pair, the link monitor enters the Link Fail state, and the transmission and reception of data packets are disabled. When a valid signal is detected on the receive pair for a minimum of 1 ms, the link monitor enters the Link Pass state, and the transmit and receive functions are enabled.

Following auto-negotiation in 1000BASE-T mode, the master transceiver begins sending data on the media. The slave transceiver also begins transmitting when it has recovered the master transceiver's timing. Each end of the link continuously monitors its local receiver status. When the local receiver status has been good for at least 1 μs, the link monitor enters the Link Pass state, and the transmission and reception of data packets are enabled. When the local receiver status is bad for more than 750 ms, the link monitor enters the Link Fail state, and the transmission and reception of data packets are then disabled.

Digital Adaptive Equalizer

The digital adaptive equalizer removes intersymbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The BCM56150 achieves an optimum signal-to-noise ratio by using a combination of feed forward equalization (FFE) and decision feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than 1×10^{-12} for transmissions of: up to 100 meters on Category 5 twisted-pair cabling for 1000BASE-T and 100BASE-TX mode; up to 100 meters on Category 3 UTP cable for 10BASE-T mode. The all-digital nature of the design makes the BCM56150 very tolerant to noise. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

Echo Canceler

Because of the bidirectional nature of the channel in 1000BASE-T, an echo impairment is caused by each transmitter. The output of the echo filter is added to the FFE output to remove the transmitted signal impairment from the incoming receive signal. The echo canceler coefficients are self-adapting to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

Crosstalk Canceler

The BCM56150 transmits and receives a continuous data stream on four channels in gigabit mode. For a given channel, the signals sent by the other three local transmitters cause impairments on the received signal because of near-end crosstalk (NEXT) between the pairs. It is possible to cancel the effect because each receiver has access to the data for the other three pairs that cause this interference. The output of the adaptive NEXT canceling filters is added to the FFE output to cancel the NEXT impairment.

Analog-to-Digital Converter

Each receive channel has its own 125 MHz analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High-power supply noise rejection
- Fast settling time
- Low bit error rate

Clock Recovery/Generator

The clock recovery and generator block creates the transmit and receive clocks for 1000BASE-T, 100BASE-TX, and 10BASE-T operation.

In 10BASE-T or 100BASE-TX mode, the transmit clock is locked to the reference clock input, and the receive clock is locked to the incoming data stream.

In 1000BASE-T mode, the two ends of the link perform loop timing. One end of the link is configured as the master, and the other is configured as the slave. The master transmit and receive clocks are locked to the reference clock input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo and NEXT impairments by ensuring that the transmitter and receiver at each end of the link are operating at the same frequency.

Baseline Wander Correction

1000BASE-T and 100BASE-TX data streams are not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can vary with data content. This effect, which is known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM56150 automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the probability of a receive symbol error.

In 10BASE-T mode, baseline wander correction is not performed because the Manchester coding provides a perfect DC balance.

Multimode TX Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits PAM5, MLT-3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high frequency signal components, reducing electromagnetic interference (EMI). The transmit DAC uses a voltage drive output that is well-balanced, and therefore, produces very low-noise transmit signals.

Stream Cipher

In 1000BASE-T and 100BASE-TX modes, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The 1000BASE-T scrambler also ensures that there is no correlation among symbols on the four different wire pairs and in the transmit and receive data streams. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require that there be no sequential or cross-channel correlation among symbols in the various data streams.

In 100BASE-TX mode, the transmit data stream is scrambled by exclusive ORing the encoded serial data stream. This is done with the output of an 11-bit wide linear feedback shift register (LFSR), producing a 2047-bit non-repeating sequence.

In 1000BASE-T mode, the transmit data stream is scrambled by exclusive ORing the input data byte with an 8-bit wide cipher text word. The cipher text word generates each symbol period from 8 uncorrelated maximal length data sequences that are produced by linear remapping of the output of a 33-bit wide LFSR. After the scrambled data bytes are encoded, the sign of each transmitted symbol is again randomized by a 4-bit wide cipher text word that is generated in the same manner as the 8-bit word. The master and slave transmitters use different scrambler sequences to generate the cipher text words. For repeater or switch applications, where all ports can transmit the same data simultaneously, signal energy is randomized further by using a unique seed to initialize the scrambler sequence for each PHY.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The BCM56150 enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that inter-packet gaps containing idles or frame extensions are received at expected intervals. When the BCM56150 detects loss of synchronization, it notifies the link partner of the inability to receive packets (1000BASE-T mode only) and attempts to resynchronize to the received data stream. If the descrambler is unable to resynchronize for a period of 750 ms, the BCM56150 is forced into the Link Fail state.

In 10BASE-T mode, scrambling is not required to reduce radiated emissions.

Wire Map and Pair Skew Correction

During 1000BASE-T operation, the BCM56150 has the ability to automatically detect and correct some UTP cable wiring errors. The symbol decoder detects and compensates for (internal to the BCM56150) the following errors:

- Wiring errors caused by the swapping of pairs within the UTP cable
- Polarity errors caused by the swapping of wires within a pair

The BCM56150 also automatically compensates for differences in the arrival times of symbols on the four pairs of the UTP cable. The varying arrival times are caused by differing propagation delays (commonly referred to as delay skew) between the wire pairs. The BCM56150 can tolerate delay skews of up to 64 ns long. Auto-negotiation must be enabled to take advantage of the wire map correction.

During 10/100Mb/s operation, pair swaps are corrected. Delay skew is not an issue though, because only one pair of wires is used in each direction.

Automatic MDI Crossover

During copper auto-negotiation, one end of the link needs to perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The BCM56150 can perform an automatic media dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports. During auto-negotiation, the BCM56150 normally transmits on TDP_[73:0]_0/TDN_[73:0]_0 and receives on TDP_[73:0]_1/TDN_[73:0]_1.

When connecting to another device that does not perform MDI crossover, the BCM56150 automatically switches its TDP_[73:0]_0/TDN_[73:0]_0 and TDP_[73:0]_1/TDN_[73:0]_1 pairs when necessary to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The MDI Crossover State can be determined by reading RDB_Register, offset 0x001, bit[13].

- 1'b0 = Normal MDI mode
- 1'b1 = Crossover MDI mode

1000BASE-T Operation

During 1000BASE-T operation, the BCM56150 swaps the transmit symbols on pairs 0 and 1 and pairs 2 and 3 if auto-negotiation completes in the MDI crossover state. The 1000BASE-T receiver automatically detects pair swaps on the receive inputs and aligns the symbols properly within the decoder. The automatic MDI crossover function can not be disabled when in 1000BASE-T mode.

10/100BASE-TX Operation (Auto-Negotiation Enabled)

During 10BASE-T and 100BASE-TX operation, pair swaps automatically occur within the device and do not require user intervention. The automatic MDI crossover function by default only works when auto-negotiation is enabled. This function can be disabled during auto-negotiation by writing to RDB_Register, offset 0x000, bit[14] = 1’b1.

10/100BASE-TX Operation (Forced Mode)

The automatic MDI crossover function can also be enabled when in forced 10BASE-T or forced 100BASE-TX mode. This feature allows the user to disable the copper auto-negotiation in either 10BASE-T or 100BASE-TX and still take advantage of the automatic MDI crossover function. This feature is enabled by writing RDB_Register, offset 0x02F, bit[9] = 1’b1.

When in forced 10BASE-T or 100BASE-TX mode, the BCM56150 has a feature that can manually swap the MDI state when the automatic MDI crossover function is disabled. Normally the BCM56150 transmits on TDP_[73:0]_[0]/TDN_[73:0]_[0] and receives on TDP_[73:0]_[1]/TDN_[73:0]_[1]. To change the MDI state to transmit on TDP_[73:0]_[1]/TDN_[73:0]_[1] and receive on TDP_[73:0]_[0]/TDN_[73:0]_[0] the following steps must be done.

- Put PHY in non-link condition.
- Enable Manual Swap MDI (Write RDB_Register, offset 0x00E, bit[7] = 1’b1).
- Set PHY into Force 10BASE-T or 100BASE-TX mode.

Note: To change the MDI state when in forced 100BASE-TX mode, the PHY must first be put into a non-link condition.

Full-Duplex Mode

The BCM56150 supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable. When auto-negotiation is disabled, full-duplex operation can be enabled by setting Register 0x00, bit[8] = 1’b1.

When auto-negotiation is enabled, full-duplex capability is advertised for:

- 10BASE-T: Register 0x04, bit[6] = 1’b1.
- 100BASE-TX: Register 0x04, bit[8] = 1’b1.
- 1000BASE-T: Register 0x09, bit[9] = 1’b1.

Master/Slave Configuration

In 1000BASE-T mode, the BCM56150 and its link partner perform loop timing. One end of the link must be configured as the timing master and the other end as the slave. Master/slave configuration is performed by the auto-negotiation function. The auto-negotiation function first looks at the manual master/slave configuration bits advertised by the local PHY and the link partner. If neither PHY requests manual configuration, then the auto-negotiation function looks at the advertised repeater/DTE settings. If one PHY is advertised as a repeater port and the other is advertised as a DTE port, then the repeater port is configured as the master and the DTE port the slave. Each end generates an 11-bit random seed if the two settings are equal; the end with the higher seed is configured as the master. If the local PHY and the link partner generate the same random seed, then auto-negotiation is restarted.

If both ends of the link attempt to force the same manual configuration (both master or both slave), or the random seeds match seven consecutive times, then the BCM56150 sets the Master/Slave Configuration Fault bit in the 1000BASE-T Status register and auto-negotiation is restarted.

For setting the BCM56150 to manual master/slave configuration or to set the advertised repeater/DTE configuration, see 1000BASE-T Control Register (Address 0x09).

Next Page Exchange

The 1000BASE-T configuration requires the exchange of three auto-negotiation next pages between the BCM56150 and its link partner. Exchange of 1000BASE-T Next Page information takes place automatically when the BCM56150 is configured to advertise 1000BASE-T capability.

The BCM56150 also supports software-controlled Next Page exchanges. When Register 0x04, bit[15] = 1’b1, all Next Page transactions are controlled through the MII management interface. This includes the three 1000BASE-T Next Pages, which are always sent first. The BCM56150 automatically generates the appropriate message code field for the 1000BASE-T pages. When the BCM56150 is not configured to advertise 1000BASE-T capability, the 1000BASE-T Next Pages are not sent.

When the BCM56150 is not configured to advertise 1000BASE-T capability and Register 0x04, bit[15] = 1’b0, the BCM56150 does not advertise Next Page ability.

Auto-Negotiation

The BCM56150, when configured to Copper mode, negotiates its mode of operation over the copper media using the auto-negotiation mechanism, defined in the IEEE 802.3u and 802.3ab specifications. When the auto-negotiation function is enabled, the BCM56150 automatically chooses the mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM56150 can be configured to advertise the following modes:

- 1000BASE-T full-duplex and/or half-duplex.
- 100BASE-TX full-duplex and/or half-duplex.
- 10BASE-T full-duplex and/or half-duplex.

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode, commonly referred to as highest common denominator (HCD). Auto-negotiation can be enabled or disabled by hardware and software control, but is always required for 1000BASE-T operation.

Ethernet@Wirespeed

Ethernet@Wirespeed is an enhancement to auto-negotiation that allows a network connection over impaired cable plants. If a link can not be established at the highest common denominator within a set number of link attempts then the BCM56150 advertises the next highest advertised speed using auto-negotiation. The set number of failed link attempts is programmable. See "Changing the Number of Failed Link Attempts" on page 66 for more details.

The BCM56150 has a link-up timer that times how long the link has been up. If the link stays up for less than 3 seconds then the Link-Fail Counter will get incremented. If the link stays up for greater than 5 seconds then the Link-Fail Counter is reset to zero.

The purpose of the link-up timer is to prevent scenarios where an unstable link (link is going up and down quickly) causes the BCM56150 to continuously try to link at a given speed and not try to downgrade and link to a lower speed. In this situation, if the link is up for less than 3 seconds, the Link-Fail Counter will get incremented. Once the Link-Fail Counter exceeds the programmable failed link attempts the BCM56150 will start advertising the next lowest speed and try to establish a link.

The link-up timer can be bypassed by setting RDB_Register, offset 0x02F, bit[10] = 1'b1. Setting this bit causes the number of failed link attempts to get reset to zero after every link up condition, no matter how short the link-up time is.

Ethernet@Wirespeed Example

At start-up the BCM56150 is advertising 1000BASE-T, 100BASE-TX, and 10BASE-T capabilities per Register 0x04 and Register 0x09 and the Link Partner is also advertising the same capabilities:

- If a link cannot be established within a programmable number of link attempts (two to nine) with 1000BASE-T being advertised then an Ethernet@Wirespeed downgrade occurs, the 1000BASE-T capability is masked out on the BCM56150 and the next highest advertised capability (100BASE-TX) is advertised.
- If a link cannot be established within a programmable number of link attempts (two to nine) with 100BASE-TX being advertised then an Ethernet@Wirespeed downgrade occurs, the 100BASE-TX is masked out on the BCM56150 and the next highest advertised capability (10BASE-T) is advertised.
- If a link can not be established within a programmable number of link attempts (two to nine) with 10BASE-T being advertised then an Ethernet@Wirespeed downgrade occurs and all advertising capabilities are enabled (1000BASE-T, 100BASE-TX, and 10BASE-T) on the BCM56150 and the whole process begins again.

Enabling/Disabling Ethernet@Wirespeed

Enabling or disabling Ethernet@Wirespeed is done on a per-port basis.

- Enable: Write RDB_Register, offset 0x02F, bit[4] = 1'b1.
- Disable: Write RDB_Register, offset 0x02F, bit[4] = 1'b0.

Removing Ethernet@Wirespeed Downgrade

Ethernet@Wirespeed downgrade can be removed by any of the following events:

- Stable link-up condition for greater than 5 seconds.
- Unplug cable (no energy) for 6 seconds.
- Hardware reset.
- Software reset (Write Register 0x00, bit[15] = 1'b1).
- Disable auto-negotiation (Write Register 0x00, bit[12] = 1'b0).
- Restart auto-negotiation (Write Register 0x00, bit[9] = 1'b1).
- Disabling Wirespeed (Write RDB_Register, offset 0x02F, bit[4] = 1'b0).
- Auto-negotiation resolves to no HCD (Highest Common Denominator).

Changing the Number of Failed Link Attempts

The number of failed link attempts before downgrading to a slower speed is programmable. The number can be programmed anywhere from two to nine failed link attempts before downgrading to a lower speed. The default value is five failed link attempts. The number of failed link attempts before downgrading to a lower speed can be programmed by writing to RDB_Register, offset 0x014, bits[4:2] as shown Table 9.

Table 9: Changing the Number of Failed Link Attempts before Downgrade

Bits[4:2]	*Description*
0x0	Number of failed link attempts before Ethernet@Wirespeed downgrade = 2
0x1	Number of failed link attempts before Ethernet@Wirespeed downgrade = 3
0x2	Number of failed link attempts before Ethernet@Wirespeed downgrade = 4
0x3	Number of failed link attempts before Ethernet@Wirespeed downgrade = 5 (Default Value)
0x4	Number of failed link attempts before Ethernet@Wirespeed downgrade = 6
0x5	Number of failed link attempts before Ethernet@Wirespeed downgrade = 7
0x6	Number of failed link attempts before Ethernet@Wirespeed downgrade = 8
0x7	Number of failed link attempts before Ethernet@Wirespeed downgrade = 9

Monitoring Ethernet@Wirespeed

The status of the Ethernet@ Wirespeed downgrade can be monitored through the following registers and LEDs.

- Ethernet@Wirespeed Downgrade Status (Read RDB_Register, offset 0x001, bit[14]).
- Ethernet@Wirespeed Downgrade (Read RDB_Register, offset 0x00C, bit[12]).
- Ethernet@Wirespeed Disable Gigabit Advertising (Read RDB_Register, offset 0x00C, bit[14]).
- Ethernet@Wirespeed Disable 100BASE-TX Advertising (Read RDB_Register, offset 0x00C, bit[13]).
- HCD Status (Read RDB_Register, offset 0x00C, bits[11:0]).
- Auto-negotiation HCD and Current Status (Read RDB_Register, offset 0x009, bits[10:8]).
- Ethernet@Wirespeed downgrade LED on LED[0] (Write RDB_Register, offset 0x01D, bits[3:0] = 0x9).
- Ethernet@Wirespeed downgrade LED on LED[1] (Write RDB_Register, offset 0x01D, bits[7:4] = 0x9).

Super Isolate Mode

When in Super Isolate mode the following happens:

- The BCM56150's transmitter and receiver on the Copper Media Dependent Interface are disabled. The link partner will go into a link down state since it is not receiving any FLPs, NLPs, or 100BASE-TX idles.

Software Enable/Disable

The BCM56150 can be put into Super Isolate mode on a per port basis by software.

- To enable Super Isolate mode:

  Write RDB_Register, offset 0x02A, bit[5] = 1'b1 for each of the 84 ports.
- To disable Super Isolate mode:

  Write RDB_Register, offset 0x02A, bit[5] = 1'b0 for each of the 84 ports.

Standby Power-Down Mode

The BCM56150 can be placed into standby Power-down mode using software commands. In this mode, all PHY functions, except for the serial management interface, are disabled. To enter standby Power-down mode, write Register 0x00, bit[11] = 1'b1. There are three ways to exit standby Power-down mode:

- Write Register 0x00, bit[11] = 1'b0 (Clear MII Control register)
- Write Register 0x00, bit[15] = 1'b1 (Software reset)
- Assert the hardware $\overline{\text{RESET}}$

Reads or writes to any MII register, other than Register 0x00 while the device is in the standby Power-down mode, returns unpredictable results. Upon exiting standby Standby Power-down mode, the BCM56150 remains in an internal reset state for 40 µs, and then resumes normal operation.

Auto Power-Down (APD) Mode

When the BCM56150 is placed into Auto Power-Down (APD) mode the chip power is reduced when the signal from the copper link partner is not present. APD mode works whether the device is in auto-negotiation enabled or in forced mode. When APD mode is enabled, the BCM56150 automatically enters the low-power mode when energy on the line is lost, and it resumes normal operation when energy is detected. When the BCM56150 is in APD mode, the copper transmitter is disabled (Sleep Cycle) for 2.7 seconds or 5.4 seconds depending on the SLEEP_TIMER_SEL bit after which the transmitter is enabled (Wake Cycle) for a duration of 84 ms to 1260 ms depending on the settings on the WAKE_UP_TIMER_SEL bits. The BCM56150 enters normal operation and establishes a link if energy is detected, otherwise, the Sleep and Wake-up cycles repeat.

ADP Mode Enable (Auto-Negotiation Enabled)

- Write RDB_Register, offset 0x01A, bits[6:5] = 2'b01.
- Write RDB_Register, offset 0x1A, bit[8] = 1'b'1.

ADP Mode Enable (Auto-Negotiation Disabled)

- Write RDB_Register, offset 0x01A, bits[6:5] = 2'b11.
- Write RDB_Register, offset 0x1A, bit[8] = 1'b'1.

ADP Mode Disable

Write RDB_Register, offset 0x01A, bits[6:5] = 2’b00.

Sleep Cycle Settings

Write RDB_Register, offset 0x01A, bit[4]

- 1’b0 = Disable copper transmitter for 2.7 seconds.
- 1’b0 = Disable copper transmitter for 5.4 seconds.

Wake Cycle Settings

Write Register RDB_Register, offset 0x01A, bits[3:0]

- 0x1 = Enable copper transmitter for 84 ms.
- 0x2 = Enable copper transmitter for 168 ms.
- 0x3 = Enable copper transmitter for 252 ms.
- 0xF = Enable copper transmitter for 1.26 seconds.

Section 6: ARM Cortex-A9 Processor Subsystem Functional Description

Cortex-A9

The Cortex-A9 processor has an integrated 32 × 32-bit single-cycle multiply/accumulate block running at CPU core speed, providing additional signal or media processing capabilities. The integrated MMU with a 128-entry TLB block allows support for common multi-threaded real-time operating systems (RTOS), such as the standard Linux® distribution.

DDR SDRAM Interface

The DDR interface is designed to be compatible with JEDEC-compliant SDRAMs. The BCM56150 supports both DDR2 and DDR3 SDRAMs. The memory interface controls main memory accesses and provides for a maximum of 2 GB of main memory.

The BCM56150 supports a variety of SDRAM configurations. Sixteen multiplexed address signals provide for device densities from 256 Mb to 8 Gb. The memory controller supports x16 configuration.

Table 10: DDR SDRAM Controller

Feature	*DDR2*	*DDR3*
SDRAM voltage	1.8V	1.5V
SDRAM clock	400 MHz	667 MHz
Data rates supported (MHz)	800 MT/s	1333 MT/s
Data bus width	16	16
Number of address bits multiplexed	16	16
Total memory supported	2 GB	2 GB
DRAM density supported	Up to 8 Gb	Up to 8 Gb

PCI Express Gen-2 Interface

The PCI Express core on the BCM56150 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the *PCI Express Base Specification v2.0*. This core contains all the necessary blocks, including logical and electrical functional subblocks, to perform PCIe functionality and maintain high-speed links using existing PCI system configuration software implementations without modification.

A configuration or link management block is provided for enumerating the PCIe configuration. The PCIe core is organized in the following logical layers:

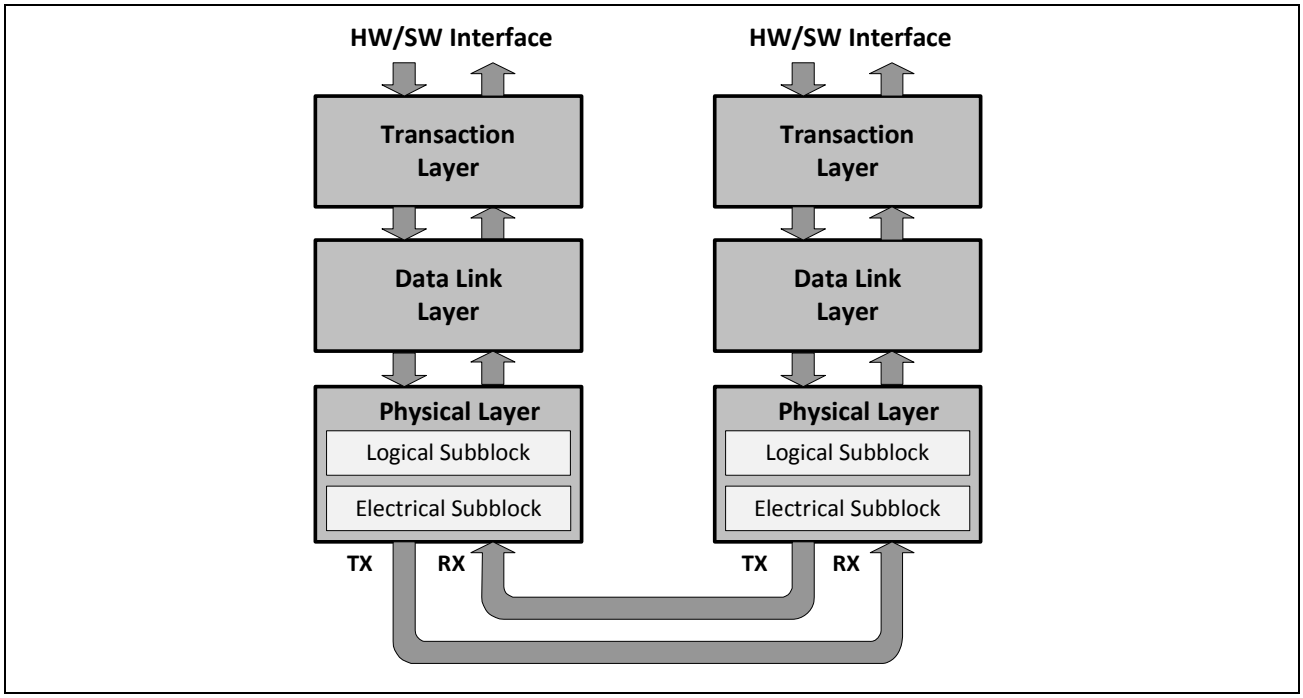
- Transaction Layer (TL)

- Data Link Layer (DLL)
- Physical Layer (PHY)

The PCIe core supports generation and reception of system management messages by communicating with the PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and BCM56150 device. The transmit side processes outbound packets while the receive side processes inbound packets. Packets are formed and generated in the transaction and data link layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields (see Figure 19).

Figure 19: PCI Express Layer Model



The BCM56150 supports one PCI Express interface that is compliant with the PCIe Gen 2 supports at 2.5GT/s or 5GT/s. This interface is configurable as root complex and also configurable as an endpoint.

The physical layer of the PCI Express interface operates at a transmission rate of 2.5 Gbps per lane. The features of the PCI Express supported are as follows:

- 1 link width supported
- Both 32-bit and 64-bit addressing, and 256-byte maximum payload size

Transaction Layer Interface

The PCIe core employs a packet-based protocol to transfer data between the host and the BCM56150 device, delivering new levels of performance and features. The upper layer of the PCIe is the transaction layer, which is primarily responsible for assembly and disassembly of Transaction Layer Packets (TLPs). TLP structure contains header, data payload, and end-to-end CRC (ECRC) fields, which are used to communicate transactions, such as read and write requests and other events.

A pipelined full split-transaction protocol is implemented in this layer to maximize efficient communication between devices with credit-based flow control of TLP, which eliminates wasted link bandwidth due to retries.

Data Link Layer

The data link layer serves as an intermediate stage between the transaction layer and the physical layer. Its primary responsibility is to provide a reliable, efficient mechanism for the exchange of TLPs between two directly connected components on the link. Services provided by the data link layer include data exchange, initialization, error detection and correction, and retry services.

Data Link Layer Packets (DLLPs) are generated and consumed by the data link layer. DLLPs are the mechanism used to transfer link management information between data link layers of the two directly connected components on the link, including TLP acknowledgement, power management, and flow control.

Physical Layer

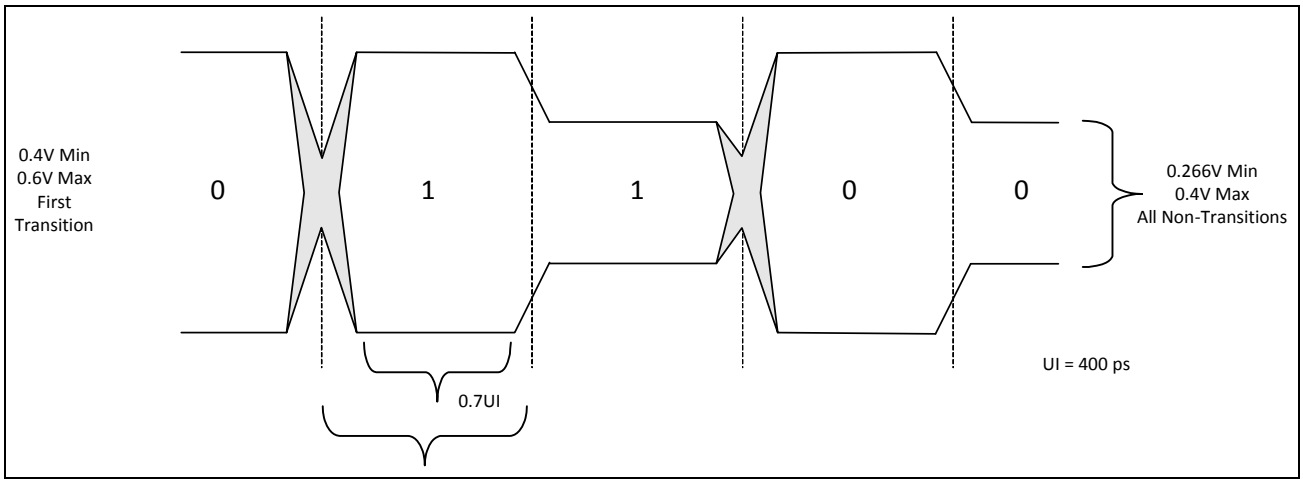
The physical layer of the PCIe provides a handshake mechanism between the data link layer and the high-speed signaling used for link data interchange. This layer is divided into the logical and electrical functional subblocks. Both subblocks have dedicated transmit and receive units that allow for point-to-point communication between the host and the PCIe device. The transmit section prepares outgoing information passed from the data link layer for transmission, and the receiver section identifies and prepares received information before passing it to the data link layer. This process involves link initialization, configuration, scrambler, and data conversion into a specific format.

Electrical Subblock

The high-speed signals utilize the Common Mode Logic (CML) signaling interface with on-chip termination and deemphasis for best in class signal integrity. A deemphasis technique is employed to reduce the effects of intersymbol interference (ISI) due to the interconnect by optimizing voltage and timing margins for worst case channel loss. This results in a maximally open “eye” at the detection point, thereby, allowing the receiver to receive data with an acceptable bit error rate (BER).

To further minimize ISI, multiple bits of the same polarity that are output in succession are deemphasized (see Figure 20). Subsequent same bits are reduced by a factor of 3.5 dB in power. This amount is specified by PCIe to allow for maximum interoperability while minimizing the complexity of controlling the deemphasis values. The high-speed interface requires AC-coupling on the transmit side to eliminate the DC common mode voltage from the receiver. The range of AC capacitance allowed is 75 nF to 200 nF.

Figure 20: Transmit Deemphasis



Configuration Space

The PCIe function in the BCM56150 implements the configuration space as defined in the PCI Express Base Specification v2.0.

NOR Serial Flash Interface

The BCM56150 has a NOR Serial Flash interface and supports Execute in Place (XIP) as a boot source configured by the strapped option.

Table 11: Serial Flash Interface

Feature	*Value*	*Comment*
Interface width	1, 2, 4	Supports single, dual, and quad SPI interfaces.
In place execute (boot support) XIP	Yes	–
Maximum number of physical devices	1	–
Extended addressing support (4B mode)	Yes	Used to address greater than 16 MB.
Devices size support	128 Mb - 4 Gb	Cannot boot from devices that support 32b addressing only. Devices that support either 24b only or mixed 24/32b addressing are supported as a boot device.
Block size	32 KB, 64 KB	–
Page sizes	2 KB, 4 KB, 8 KB	–
Maximum frequency	62.5 MHz	–
NOR Flash support	Yes	Some Serial Flash in the managed NAND Flash that appears as a NOR.

NOR Parallel Flash Interface

The BCM56150 has a NOR parallel Flash interface and supports Execute in Place (XIP) as a boot source configured by the strapped option. The BCM56150 provides two chip select signals supporting Parallel NORFlash devices or any local bus devices that are compliant with Parallel NOR Flash Interface timing.

Table 12: Parallel NOR Flash Interface

Feature	*Value*	*Comment*
Interface width	8-bit or 16-bit	–
In place execute (boot support) XIP	Yes	–
Maximum number of physical devices	2	Two chip selects Can only boot from device connected to IP_PFLASH_CS0_L
Total Memory Support	64 MB	–
Address bus	25b	25 address bits for x8 device 24 address bits for x16 device
Devices size support	128 Mb - 256 Mb	Cannot boot from devices that support 32b addressing only. Devices that support either 24b only or mixed 24/32b addressing are supported as a boot device.
Block size	32K, 64K	–
Page sizes	2K, 4K, 8K	–
Maximum frequency	62.5 MHz	–

NAND Flash Interface

The BCM56150 is Open NAND Flash Interface (ONFI) compliant with the NAND Flash interface, supporting single-level cell (SLC)/multi-level cell (MLC) devices and with on-chip error-correction code (ECC). The interface can be configured as a boot source by the strapped configuration. The BCM56150 provides two NAND flash chip select signals, but only IP_PFLASH_CS0_L can be configured as a boot source.

Table 13: NAND Flash Interface Features

Feature	*Value*	*Comment*
NAND Flash support	SLC/MLC	–
ONFI Interface async	8-bit or 16-bit	Version 2.2 compliant
ONFI interface sync	No	–
Hardware ECC	Yes	1-bit Hamming and 1-40bit BCH codes
SLC Flash support	Yes	–
MLC Flash support	Yes	–
ECC–Hamming: Single bit correction, double bit detection	Yes	–
BCH–ECC size (512B Block)	4, 8, 12, 15	–

Table 13: NAND Flash Interface Features (Cont.)

Feature	*Value*	*Comment*
BCH–ECC size (1024B Block)	24-40	–
Async Timing modes	Modes 0-5	Boots in Mode 0. Mode 4 and 5 are EDO capable.
In place execute (boot support) XIF	yes	–
Maximum number of physical devices	2	Two chip selects
Total Memory Support	32 MB	32 MB for direct access. For indirect access, the capacity is limited only by device availability and not by the controller.
Devices Size Support	128 Mb–256 Mb	–
Block Size	8K, 16K, 128K, 256K, 512K	–
Page Sizes	2K, 4K, 8K	NAND boot supported for 2K, 4K and 8K page sizes only.
Signaling	1.8V/3.3V	Supports these interface voltage levels.
FLASH power supply	1.8V/3.3V	–

MIIM/UART/GPIO Interfaces

The BCM56150 supports:

- Three MDC/MDIO interfaces.
- One UART1 interface with CTS and RTS signals.
- One dedicated two-wire UART2 interface (UART2 TX and UART2 RX pins)
- Sixteen 3.3V GPIO pins that can be used to connect to various external devices.

SPI interface

SPI is a serial interface that is compatible with a subset of the Motorola Synchronous Serial Peripheral Interconnect (SPI) bus. The SPI interface can be configured to operate in either master or slave mode. The SPI interface consists of a set of four signals:

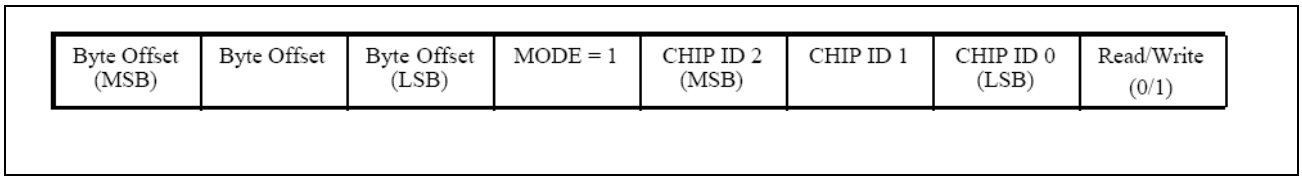
- Serial clock (SCK)
- Slave select (SS_L)
- Master-in/slave-out (MISO)
- Master-out/slave-in (MISI)

When the SPI interface operates as an SPI slave device, in that it never initiates a transfer and allows external master to read and write to various internal register spaces and memory tables of the chip. During a transaction, data is captured on the rising edge of SCK and propagated at the falling edge of SCK. This corresponds to the modes 0 (SPO = 0 and SPH = 0) and 3 (SPO = 1 and SPH = 1) of the Motorola SPI format.

A layer of protocol is added to the basic SPI definition to facilitate data transfers from the chip. This protocol establishes the definition of the first two bytes issued by the external master to the SPI slave during a transfer. The first byte issued from the master in any transaction is defined as a command byte, which is always followed by a register address byte, and any additional address bytes and data bytes.

The SPI interface supports the fast SPI access mechanisms, determined by the content of the command byte. Figure 21 shows the fast SPI command byte.

Figure 21: Fast SPI Command Byte



In a fast command byte, the Mode bit (bit [4]) of the command byte is a 1. Bits [7:5] indicate the byte offset into the register that the access starts from and bits [3:0] indicate the Chip ID to be accessed. Bit 0 of the command byte is the Read/Write signal (0= Read, 1= Write) that determines the data direction for the transaction.

The 4 bytes following the command byte are register address bytes. The register address is 32 bits wide. The lower byte of the address is transmitted first, followed by the higher bytes.

In case of a write command, 4 data bytes follow the write address. As in the case of address, the lower byte is transmitted first. A write transaction is initiated once all the address and data bytes are received.

All write operations are of the form:

<CMD, CHIP_ID, W><REG ADDR0> <REG ADDR1><REG ADDR2><REG ADDR3><DATA0><DATA1><DATA2><DATA3>

In case of a read command, a read transaction is initiated once all the address bytes are received. The data received back from the chip is transmitted as the read response to the master.

All read operations are of the form:

<CMD, CHIP_ID, R><REG ADDR0><REG ADDR1>><REG ADDR2><REG ADDR3>

SPI slave runs in Fast SPI mode. In Fast SPI mode, the SPI slave returns the ACK bit before transmitting the read data. The ACK bit is transferred as the LSB of each byte. Till the time the read access is on progress, SPI will return 0x00 on the MISO line. Once read data is available, SPI returns 0x01 followed by 4 bytes of read data.

MII Interface

The BCM56150 includes a Media Independent Interface (MII) supporting auto-negotiation:

- 100 Mbps half- and full-duplex operation
- 10 Mbps half- and full-duplex operation

The BCM56150 interfaces to external physical media devices supporting the MII specification for 10/100 Mbps operation.

The MII interface pins use LVTTL buffers and operates at 3.3V. Table shows MII to media connection for several interfacing schemes (see Table 14).

Table 14: Alternative MII Interface Signals

Signal	*MII (at 10 Mbit)*	*MII (at 100 Mbit)*
RXD[3:0]	RXD[3:0]	RXD[3:0]
RXDV	RXDV	RXDV
RXER	RXER	RXER
CRS	CRS	CRS
COL	COL	COL
TXC	TXC (2.5 MHz)	TXC (25 MHz)
TXD[3:0]	TXD[3:0]	TXD[3:0]
TXEN	TXEN	TXEN
TXER	TXER	TXER

Section 7: Pin List Description

Signal Name Descriptions

Note: This is a preliminary pin assignment and is subject to change.

The section describes the BCM56150 hardware signals. The following conventions are used:

- I = Input signal
- O = Output signal
- B = Bidirectional signal
- BOD = Open-drain bidirectional signal
- BPU =Bidirectional signal with internal pull-up
- IPD = Input signal with internal pull-down
- IPU = Input signal with internal pull-up
- OOD = Open-drain output
- P = Power

Table 15: BCM56150 Hardware Signals

Pin Names	*Quantity*	*I/O*	*V*	*Pin Description*
GPIO				
GPIO[15:0]	16	I/O	3.3V	General-purpose I/O • GPIO15 shared with RXER, LED_P7_2 • GPIO14 shared with RXDV, LED_P6_2 • GPIO13 shared with RXD3, LED_P5_2 • GPIO12 shared with RXD2, LED_P4_2 • GPIO11 shared with RXD1, LED_P3_2 • GPIO10 shared with RXD0, LED_P2_2 • GPIO9 shared with TXC, LED_P1_2 • GPIO8 shared with RXC, LED_P0_2 • GPIO[7:0] are dedicated pins and GPIO[3:0] are time stamp capable. ***Note:*** GPIO[3:0] can be reset by resetting SYS_RST_L. GPIO[15:4] are reset only on power-on and cannot be reset by just doing the software chip reset alone.
UART Port 1				
UART1_RX	1	I_{PD}	3.3V	UART port 1 Receive data input

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	Quantity	I/O	V	Pin Description
UART1_TX	1	O	3.3V	UART port 1 Transmit data output.
UART1_CTS_L	1	I_{PU}	3.3V	UART port 1Clear to Send
UART1_RTS_L	1	O	3.3V	UART port 1Request to Send Shared with SFLASH_BYTE_ADDR
UART1_DTR_L	1	O	3.3V	UART port 1 Data Terminal Ready
UART1_DCD_L	1	I_{PU}	3.3V	UART port 1 Data Carrier Detect
UART1_DSR_L	1	I_{PU}	3.3V	UART port 1 Data Set Ready
UART1_RI_L	1	I_{PU}	3.3V	UART port 1 Ring Indicator
UART Port 2				
UART2_RX	1	I_{PD}	3.3V	UART port 2receive data input
UART2_TX	1	O	3.3V	UART port 2transmit data output.
SPI Port				
SCK	1	I/O	3.3V	Serial Port Interface Clock. This clock output is driven low during idle in master mode. In slave mode it is the clock input to the serial port interface supplied by the SPI master. Shared with LED_P8_2, CRS
MISO	1	I/O	3.3V	Master-In/Slave-Out. Output signal driven with serial data during a serial port interface Read operations. Shared with LED_P9_2, COL
MOSI	1	I/O	3.3V	Master-Out/Slave-In. This output is driven low during idle in master mode. In slave mode it is the input signal which receives control and address information for the serial port interface, as well as serial data during Write operations. Shared with LED_P10_2, TXD0
SS_L	1	I/O	3.3V	Slave Select. This output is driven high during idle in master mode. In slave mode it is an active low signal that enables a serial port interface Read or Write operations. Shared with LED_P11_2, TXD1
QSPI FLASH Interface				
SFLASH_CLK	1	O	3.3V	SPI flash clock This clock output is driven high during idle.
SFLASH_CS_L	1	I/O	3.3V	External SPI flash chip select This chip select is driven high during idle.

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	*Quantity*	*I/O*	*V*	*Pin Description*
SFLASH_IO0	1	I/O	3.3V	SFLASH_IO_0: • SINGLE-SPI flash DO or MOSI • DUAL-SPI flash IO0 • QUAD-SPI flash IO0 This output is driven low during idle.
SFLASH_IO1	1	I_{PD}/ O_{PD}	3.3V	SFLASH_IO_1: • SINGLE-SPI flash DI or MISO • DUAL-SPI flash IO1 • QUAD-SPI flash IO1
SFLASH_IO2	1	I/O	3.3V	SFLASH_IO_2: • SINGLE-SPI flash WP_L • DUAL-SPI flash WP_L • QUAD-SPI flash IO2 This output is driven high during idle.
SFLASH_IO3	1	I/O	3.3V	SFLASH_IO_3: • SINGLE-SPI flash HOLD_L • DUAL-SPI flash HOLD_L • QUAD-SPI flash IO3 This output is driven high during idle.
PARALLEL FLASH Interface				
IP_PFLASH_DATA[15:0]	16	I/O	3.3V	Parallel Flash Data Out
IP_PFLASH_CS0_L	1	O	3.3V	Parallel Flash Chip Select 0
IP_PFLASH_CS1_L	1	O	3.3V	Parallel Flash Chip Select 1
IP_PFLASH_REN_L	1	O	3.3V	Parallel Flash Read Enable
IP_PFLASH_WEN_L	1	O	3.3V	Parallel Flash Write Enable
IP_PFLASH_RB_L	1	$I_{OD/PU}$	3.3V	Parallel NAND Flash Ready Busy
IP_PFLASH_WP_L	1	O	3.3V	Parallel NAND Flash Write Protection Shared with IP_PFLASH_AD1
IP_PFLASH_ALE	1	O	3.3V	Parallel NAND Flash Address Latch Enable Shared with IP_PFLASH_AD14
IP_PFLASH_CLE	1	O	3.3V	Parallel NAND Flash Command Latch Enable Shared with IP_PFLASH_AD15

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	*Quantity*	*I/O*	*V*	*Pin Description*
IP_PFLASH_AD[24:0]	25	O	3.3V	Parallel Flash Address Bus: • IP_PFLASH_AD24 shared with IP_DDR_TYPE • IP_PFLASH_AD20 shared with NAND_DATA_WIDTH • IP_PFLASH_AD15 shared with IP_PFLASH_CLE • IP_PFLASH_AD14 shared with IP_PFLASH_ALE • IP_PFLASH_AD[13:12] shared with NOR_MEM_WIDTH[1:0] pins • IP_PFLASH_AD[11:10] shared with NAND_PAGE[1:0] pins • IP_PFLASH_AD[9:6] shared with NAND_TYPE[3:0] pins • IP_PFLASH_AD5 shared with PCIE_FORCE_GEN1 • IP_PFLASH_AD4 shared with PCIE_REFCLK_SEL • IP_PFLASH_AD3 shared with PCIE_RC_MODE • IP_PFLASH_AD2 shared with PCIE_IF_ENABLE • IP_PFLASH_AD1 shared with IP_PFLASH_WP_L
Parallel LED Interface				
LED_P0_[2:0]	3	O	3.3V	Per Port Parallel LED Indicators
LED_P1_[2:0]	3	O	3.3V	LED_P0_2 shared with RXC, GPIO8
LED_P2_[2:0]	3	O	3.3V	LED_P1_2 shared with TXC, GPIO9
LED_P3_[2:0]	3	O	3.3V	LED_P2_2 shared with RXD0, GPIO10
LED_P4_[2:0]	3	O	3.3V	LED_P3_2 shared with RXD1, GPIO11
LED_P5_[2:0]	3	O	3.3V	LED_P4_2 shared with RXD2, GPIO12
LED_P6_[2:0]	3	O	3.3V	LED_P5_2 shared with RXD3, GPIO13
LED_P7_[2:0]	3	O	3.3V	LED_P6_2 shared with RXDV, GPIO14
LED_P8_[2:0]	3	O	3.3V	LED_P7_2 shared with RXER, GPIO15
LED_P9_[2:0]	3	O	3.3V	LED_P8_2 shared with CRS, SCK
LED_P10_[2:0]	3	O	3.3V	LED_P9_2 shared with COL, MISO
LED_P11_[2:0]	3	O	3.3V	LED_P10_2 shared with TXD0, MOSI
LED_P12_[2:0]	3	O	3.3V	LED_P11_2 shared with TXD1, SS_L
LED_P13_[2:0]	3	O	3.3V	LED_P12_2 shared with TXD2
LED_P14_[2:0]	3	O	3.3V	LED_P13_2 shared with TXD3
LED_P15_[2:0]	3	O	3.3V	LED_P14_2 shared with TXEN
				LED_P15_2 shared with TXER
Serial LED Interface				
LED_CLK	1	O	3.3V	Serial LED clock output
LED_DATA	1	O	3.3V	Serial LED data output Shared with EXT_UC_IS_SPI
Strap Pins				

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	*Quantity*	*I/O*	*V*	*Pin Description*
OSC_XTAL_SEL	1	I_{PU}	3.3V	Select External 25 MHz Oscillator or Crystal for system clock source 0: Use External Oscillator 1: Use External Crystal (Default)
EXT_UC_PRESENT	1	I_{PD}	3.3V	[EXT_UC_PRESENT, EXT_UC_IS_SPI] • [0, x]: SPI master mode and BSC master mode • [1, 0]: SPI master mode and BSC slave mode • [1, 1]: SPI slave mode and BSC master mode EXT_UC_IS_SPI shared wIth LED_DATA
EXT_UC_IS_SPI	1	I_{PD}	3.3V	
IP_DDR_TYPE	1	I_{PU}	3.3V	DDR Type/Voltage Selection: • 1: DDR3 (1.5V) • 0: DDR2 (1.8V) Shared with IP_PFLASH_AD24
NAND_DATA_WIDTH	1	I_{PU}	3.3V	Parallel NAND Flash Data Width • 0: 8 bit • 1: 16 bit (Default) Share with IP_PFLASH_AD20
NOR_MEM_WIDTH[1] NOR_MEM_WIDTH[0]	2	I_{PD} I_{PU}	3.3V	Parallel NOR Flash Memory Width • 0: 8 bit • 1: 16 bit (Default) • 2: Reserved • 3: Reserved Share with IP_PFLASH_AD13 and IP_PFLASH_AD12 pins
NAND_PAGE[1:0]	2	I_{PD}	3.3V	NAND Page Size • 0: 2 KB page, 4 address cycles (Default) • 1: 2 KB page, 5 address cycles • 2: 4 KB page, 5 address cycles • 3: 8 KB page, 5 address cycles Shared with IP_PFLASH_AD11 and IP_PFLASH_AD10 pins

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	Quantity	I/O	V	Pin Description
NAND_TYPE[3:0]	4	I_{PD}	3.3V	NAND Type 4b'0000 - NAND + ECC disabled & 16B-spare- 512B sector (Default) 4b'0001 - NAND + 1 bit ECC & 16B-spare - 512B sector 4b'0010 - NAND + 4 bit ECC & 16B-spare - 512B sector 4b'0011 - NAND + 8 bit ECC & 16B-spare - 512B sector 4b'0100 - NAND + 8 bit ECC & 27B-spare - 512B sector 4b'0101 - NAND + 12 bit ECC & 27B-spare - 512B sector 4b'0110 - NAND + 24 bit ECC & 54B-spare - 1 KB sector 4b'0111 - NAND + 30 bit ECC & 54B-spare - 1 KB sector 4b'1000 - NAND + 40 bit ECC & 90B-spare - 1 KB sector Shared with IP_PFLASH_AD9, IP_PFLASH_AD8, IP_PFLASH_AD7 and IP_PFLASH_AD6 pins
PCIE_FORCE_GEN1	1	I_{PD}	3.3V	Force PCIe GEN 1 Compliant • 0: GEN 2 mode (Default) • 1: Force GEN 1 compliant Shared with IP_PFLASH_AD5
PCIE_REFCLK_SEL	1	I_{PU}	3.3V	PCIe Interface Clock Source Control • 0: Select external clock source from PCIE_REFCLKP/N input • 1: Use on-chip internal clock source (Default) Shared with IP_PFLASH_AD4
PCIE_RC_MODE	1	I_{PD}	3.3V	Configures the PCI Express interface(s) to operate as a Root Complex or End Point: • 0: The PCIe interface is operating as an End Point. • 1: The PCIe interface is operating as a Root Complex. And the PCIE_CLKOUTP/N are an output clock for driving external EP device. Shared with IP_PFLASH_AD3
PCIE_IF_ENABLE	1	I_{PD}	3.3V	Enable PCIe Interface • 0: PCIe interface is disabled (Default) • 1: Enable PCIe interface Shared with IP_PFLASH_AD2

Table 15: BCM56150 Hardware Signals (Cont.)

<table>
<tr><th>Pin Names</th><th>Quantity</th><th>I/O</th><th>V</th><th>Pin Description</th></tr>
<tr><td>IP_BOOT_DEV2</td><td>1</td><td>I_{PD}</td><td>3.3V</td><td rowspan="3">IP_BOOT_DEV[2:0]
CPU ARM boot device selection:
• 3'b000 - SPI-NOR Flash (BSPI/QSPI)
• 3'b001 - NAND Flash
• 3'b010 - Reserved
• 3'b011 - Reserved
• 3'b100 - Parallel NOR Flash
Configures also the following address bus:
<table><tr><th>IP_BOOT_DEV[2:0]</th><th>IP_PFLASH_AD1/WP_L</th><th>IP_PFLASH_AD14/ALE</th><th>IP_PFLASH_AD15/CLE</th></tr><tr><td>3’b100</td><td>IP_PFLASH_AD1</td><td>IP_PFLASH_AD14</td><td>IP_PFLASH_AD15</td></tr><tr><td>3’b0xx</td><td>IP_PFLASH_WP_L</td><td>IP_PFLASH_ALE</td><td>IP_PFLASH_CLE</td></tr></table></td></tr>
<tr><td>IP_BOOT_DEV1</td><td>1</td><td>I_{PD}</td><td>3.3V</td></tr>
<tr><td>IP_BOOT_DEV0</td><td>1</td><td>I_{PD}</td><td>3.3V</td></tr>
<tr><td>LED_MII_GPIO-SPI_SEL[1:0]</td><td>2</td><td>I_{PD}</td><td>3.3V</td><td>Select LED/MII/GPIO-SPI Function
• 0: LED Mode
• 1: MII Mode
• 2: GPIO-SPI Mode
• 3: Reserved</td></tr>
<tr><td>SFLASH_BYTE_ADDR</td><td>1</td><td>I_{PU}</td><td>3.3V</td><td>SFLASH Byte Address
• 0: 4 byte address
• 1: 3 byte address
Shared with UART1_RTS_L</td></tr>
<tr><td>PCIe Port</td><td></td><td></td><td></td><td></td></tr>
<tr><td>PCIE_INTR_L</td><td>1</td><td>O_{PU}</td><td>3.3V</td><td>PCIe Interrupt</td></tr>
<tr><td>PCIE_PERST_L</td><td>1</td><td>I_{PU}/ O_{PU}</td><td>3.3V</td><td>PCIe port reset (active low):
• Output in RC mode
• Input in EP mode</td></tr>
<tr><td>PCIE_PME_WAKE_L</td><td>1</td><td>$I_{OD/PU}$ $O_{OD/PU}$</td><td>3.3V</td><td>PCIe port power management event (Open Drain with internal pulled up).</td></tr>
<tr><td>PCIE_RDN</td><td>1</td><td>I</td><td>1.0V</td><td>Negative leg of the differential pair receive serial data on PCIe port.</td></tr>
<tr><td>PCIE_RDP</td><td>1</td><td>I</td><td>1.0V</td><td>Positive leg of the differential pair receive serial data on PCIe port.</td></tr>
<tr><td>PCIE_TDP</td><td>1</td><td>O</td><td>1.0V</td><td>Positive leg of the differential pair transmit serial data on PCIe port.</td></tr>
<tr><td>PCIE_TDN</td><td>1</td><td>O</td><td>1.0V</td><td>Negative leg of the differential pair transmit serial data on PCIe port.</td></tr>
<tr><td>PCIE_CLKOUTN</td><td>1</td><td>O</td><td>1.0V</td><td>Negative leg of 100 MHz reference clock output differential pair for external EP device in RC mode.</td></tr>
</table>

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	*Quantity*	*I/O*	*V*	*Pin Description*
PCIE_CLKOUTP	1	O	1.0V	Positive leg of 100 MHz reference clock output differential pair for external EP device in RC mode.
PCIE_REFCLKN	1	I	1.0V	Negative leg of 100 MHz reference clock input differential pair for PCIe port in EP mode.
PCIE_REFCLKP	1	I	1.0V	Positive leg of 100 MHz reference clock input differential pair for PCIe port in EP mode.
Clock Input				
XTALN	1	I	1.0V	25M crystal differential input negative leg.
XTALP	1	I	1.0V	25M crystal differential input positive leg.
JTAG Interface				
JTCK	1	I_{PD}	3.3V	JTAG test clock
JTDO	1	O	3.3V	JTAG test data output
JTMS	1	I_{PU}	3.3V	JTAG mode select
JTRST	1	I_{PU}	3.3V	JTAG reset Must be pulled low during normal switch operation.
JTDI	1	I_{PU}	3.3V	JTAG test data input
JTCE1, JTCE	2	I_{PD}	3.3V	JTAG test enable [JTCE1, JTCE] 1X: JTAG Mode 01: ARM Debug Mode 00: Normal Mode Must be pulled low during normal switch operation.
SWITCH GPHY Port 0-15				
GP0_TD0P	1	I_A/O_A	1.0V	Port 0 pair 0 positive leg
GP0_TD0N	1	I_A/O_A	1.0V	Port 0 pair 0 negative leg
GP0_TD1P	1	I_A/O_A	1.0V	Port 0 pair 1 positive leg
GP0_TD1N	1	I_A/O_A	1.0V	Port 0 pair 1 negative leg
GP0_TD2P	1	I_A/O_A	1.0V	Port 0 pair 2 positive leg
GP0_TD2N	1	I_A/O_A	1.0V	Port 0 pair 2 negative leg
GP0_TD3P	1	I_A/O_A	1.0V	Port 0 pair 3 positive leg
GP0_TD3N	1	I_A/O_A	1.0V	Port 0 pair 3 negative leg
GP1_TD0P	1	I_A/O_A	1.0V	Port 1 pair 0 positive leg
GP1_TD0N	1	I_A/O_A	1.0V	Port 1 pair 0 negative leg
GP1_TD1P	1	I_A/O_A	1.0V	Port 1 pair 1 positive leg
GP1_TD1N	1	I_A/O_A	1.0V	Port 1 pair 1 negative leg
GP1_TD2P	1	I_A/O_A	1.0V	Port 1 pair 2 positive leg
GP1_TD2N	1	I_A/O_A	1.0V	Port 1 pair 2 negative leg
GP1_TD3P	1	I_A/O_A	1.0V	Port 1 pair 3 positive leg

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	*Quantity*	*I/O*	*V*	*Pin Description*
GP1_TD3N	1	I_A/O_A	1.0V	Port 1 pair 3 negative leg
GP2_TD0P	1	I_A/O_A	1.0V	Port 2 pair 0 positive leg
GP2_TD0N	1	I_A/O_A	1.0V	Port 2 pair 0 negative leg
GP2_TD1P	1	I_A/O_A	1.0V	Port 2 pair 1 positive leg
GP2_TD1N	1	I_A/O_A	1.0V	Port 2 pair 1 negative leg
GP2_TD2P	1	I_A/O_A	1.0V	Port 2 pair 2 positive leg
GP2_TD2N	1	I_A/O_A	1.0V	Port 2 pair 2 negative leg
GP2_TD3P	1	I_A/O_A	1.0V	Port 2 pair 3 positive leg
GP2_TD3N	1	I_A/O_A	1.0V	Port 2 pair 3 negative leg
GP3_TD0P	1	I_A/O_A	1.0V	Port 3 pair 0 positive leg
GP3_TD0N	1	I_A/O_A	1.0V	Port 3 pair 0 negative leg
GP3_TD1P	1	I_A/O_A	1.0V	Port 3 pair 1 positive leg
GP3_TD1N	1	I_A/O_A	1.0V	Port 3 pair 1 negative leg
GP3_TD2P	1	I_A/O_A	1.0V	Port 3 pair 2 positive leg
GP3_TD2N	1	I_A/O_A	1.0V	Port 3 pair 2 negative leg
GP3_TD3P	1	I_A/O_A	1.0V	Port 3 pair 3 positive leg
GP3_TD3N	1	I_A/O_A	1.0V	Port 3 pair 3 negative leg
GP4_TD0P	1	I_A/O_A	1.0V	Port 4 pair 0 positive leg
GP4_TD0N	1	I_A/O_A	1.0V	Port 4 pair 0 negative leg
GP4_TD1P	1	I_A/O_A	1.0V	Port 4 pair 1 positive leg
GP4_TD1N	1	I_A/O_A	1.0V	Port 4 pair 1 negative leg
GP4_TD2P	1	I_A/O_A	1.0V	Port 4 pair 2 positive leg
GP4_TD2N	1	I_A/O_A	1.0V	Port 4 pair 2 negative leg
GP4_TD3P	1	I_A/O_A	1.0V	Port 4 pair 3 positive leg
GP4_TD3N	1	I_A/O_A	1.0V	Port 4 pair 3 negative leg
GP5_TD0P	1	I_A/O_A	1.0V	Port 5 pair 0 positive leg
GP5_TD0N	1	I_A/O_A	1.0V	Port 5 pair 0 negative leg
GP5_TD1P	1	I_A/O_A	1.0V	Port 5 pair 1 positive leg
GP5_TD1N	1	I_A/O_A	1.0V	Port 5 pair 1 negative leg
GP5_TD2P	1	I_A/O_A	1.0V	Port 5 pair 2 positive leg
GP5_TD2N	1	I_A/O_A	1.0V	Port 5 pair 2 negative leg
GP5_TD3P	1	I_A/O_A	1.0V	Port 5 pair 3 positive leg
GP5_TD3N	1	I_A/O_A	1.0V	Port 5 pair 3 negative leg
GP6_TD0P	1	I_A/O_A	1.0V	Port 6 pair 0 positive leg
GP6_TD0N	1	I_A/O_A	1.0V	Port 6 pair 0 negative leg

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	*Quantity*	*I/O*	*V*	*Pin Description*
GP6_TD1P	1	I_A/O_A	1.0V	Port 6 pair 1 positive leg
GP6_TD1N	1	I_A/O_A	1.0V	Port 6 pair 1 negative leg
GP6_TD2P	1	I_A/O_A	1.0V	Port 6 pair 2 positive leg
GP6_TD2N	1	I_A/O_A	1.0V	Port 6 pair 2 negative leg
GP6_TD3P	1	I_A/O_A	1.0V	Port 6 pair 3 positive leg
GP6_TD3N	1	I_A/O_A	1.0V	Port 6 pair 3 negative leg
GP7_TD0P	1	I_A/O_A	1.0V	Port 7 pair 0 positive leg
GP7_TD0N	1	I_A/O_A	1.0V	Port 7 pair 0 negative leg
GP7_TD1P	1	I_A/O_A	1.0V	Port 7 pair 1 positive leg
GP7_TD1N	1	I_A/O_A	1.0V	Port 7 pair 1 negative leg
GP7_TD2P	1	I_A/O_A	1.0V	Port 7 pair 2 positive leg
GP7_TD2N	1	I_A/O_A	1.0V	Port 7 pair 2 negative leg
GP7_TD3P	1	I_A/O_A	1.0V	Port 7 pair 3 positive leg
GP7_TD3N	1	I_A/O_A	1.0V	Port 7 pair 3 negative leg
GP8_TD0P	1	I_A/O_A	1.0V	Port 8 pair 0 positive leg
GP8_TD0N	1	I_A/O_A	1.0V	Port 8 pair 0 negative leg
GP8_TD1P	1	I_A/O_A	1.0V	Port 8 pair 1 positive leg
GP8_TD1N	1	I_A/O_A	1.0V	Port 8 pair 1 negative leg
GP8_TD2P	1	I_A/O_A	1.0V	Port 8 pair 2 positive leg
GP8_TD2N	1	I_A/O_A	1.0V	Port 8 pair 2 negative leg
GP8_TD3P	1	I_A/O_A	1.0V	Port 8 pair 3 positive leg
GP8_TD3N	1	I_A/O_A	1.0V	Port 8 pair 3 negative leg
GP9_TD0P	1	I_A/O_A	1.0V	Port 9 pair 0 positive leg
GP9_TD0N	1	I_A/O_A	1.0V	Port 9 pair 0 negative leg
GP9_TD1P	1	I_A/O_A	1.0V	Port 9 pair 1 positive leg
GP9_TD1N	1	I_A/O_A	1.0V	Port 9 pair 1 negative leg
GP9_TD2P	1	I_A/O_A	1.0V	Port 9 pair 2 positive leg
GP9_TD2N	1	I_A/O_A	1.0V	Port 9 pair 2 negative leg
GP9_TD3P	1	I_A/O_A	1.0V	Port 9 pair 3 positive leg
GP9_TD3N	1	I_A/O_A	1.0V	Port 9 pair 3 negative leg
GP10_TD0P	1	I_A/O_A	1.0V	Port 10 pair 0 positive leg
GP10_TD0N	1	I_A/O_A	1.0V	Port 10 pair 0 negative leg
GP10_TD1P	1	I_A/O_A	1.0V	Port 10 pair 1 positive leg
GP10_TD1N	1	I_A/O_A	1.0V	Port 10 pair 1 negative leg
GP10_TD2P	1	I_A/O_A	1.0V	Port 10 pair 2 positive leg

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	*Quantity*	*I/O*	*V*	*Pin Description*
GP10_TD2N	1	I_A/O_A	1.0V	Port 10 pair 2 negative leg
GP10_TD3P	1	I_A/O_A	1.0V	Port 10 pair 3 positive leg
GP10_TD3N	1	I_A/O_A	1.0V	Port 10 pair 3 negative leg
GP11_TD0P	1	I_A/O_A	1.0V	Port 11 pair 0 positive leg
GP11_TD0N	1	I_A/O_A	1.0V	Port 11 pair 0 negative leg
GP11_TD1P	1	I_A/O_A	1.0V	Port 11 pair 1 positive leg
GP11_TD1N	1	I_A/O_A	1.0V	Port 11 pair 1 negative leg
GP11_TD2P	1	I_A/O_A	1.0V	Port 11 pair 2 positive leg
GP11_TD2N	1	I_A/O_A	1.0V	Port 11 pair 2 negative leg
GP11_TD3P	1	I_A/O_A	1.0V	Port 11 pair 3 positive leg
GP11_TD3N	1	I_A/O_A	1.0V	Port 11 pair 3 negative leg
GP12_TD0P	1	I_A/O_A	1.0V	Port 12 pair 0 positive leg
GP12_TD0N	1	I_A/O_A	1.0V	Port 12 pair 0 negative leg
GP12_TD1P	1	I_A/O_A	1.0V	Port 12 pair 1 positive leg
GP12_TD1N	1	I_A/O_A	1.0V	Port 12 pair 1 negative leg
GP12_TD2P	1	I_A/O_A	1.0V	Port 12 pair 2 positive leg
GP12_TD2N	1	I_A/O_A	1.0V	Port 12 pair 2 negative leg
GP12_TD3P	1	I_A/O_A	1.0V	Port 12 pair 3 positive leg
GP12_TD3N	1	I_A/O_A	1.0V	Port 12 pair 3 negative leg
GP13_TD0P	1	I_A/O_A	1.0V	Port 13 pair 0 positive leg
GP13_TD0N	1	I_A/O_A	1.0V	Port 13 pair 0 negative leg
GP13_TD1P	1	I_A/O_A	1.0V	Port 13 pair 1 positive leg
GP13_TD1N	1	I_A/O_A	1.0V	Port 13 pair 1 negative leg
GP13_TD2P	1	I_A/O_A	1.0V	Port 13 pair 2 positive leg
GP13_TD2N	1	I_A/O_A	1.0V	Port 13 pair 2 negative leg
GP13_TD3P	1	I_A/O_A	1.0V	Port 13 pair 3 positive leg
GP13_TD3N	1	I_A/O_A	1.0V	Port 13 pair 3 negative leg
GP14_TD0P	1	I_A/O_A	1.0V	Port 14 pair 0 positive leg
GP14_TD0N	1	I_A/O_A	1.0V	Port 14 pair 0 negative leg
GP14_TD1P	1	I_A/O_A	1.0V	Port 14 pair 1 positive leg
GP14_TD1N	1	I_A/O_A	1.0V	Port 14 pair 1 negative leg
GP14_TD2P	1	I_A/O_A	1.0V	Port 14 pair 2 positive leg
GP14_TD2N	1	I_A/O_A	1.0V	Port 14 pair 2 negative leg
GP14_TD3P	1	I_A/O_A	1.0V	Port 14 pair 3 positive leg
GP14_TD3N	1	I_A/O_A	1.0V	Port 14 pair 3 negative leg

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	Quantity	I/O	V	Pin Description
GP15_TD0P	1	I_A/O_A	1.0V	Port 15 pair 0 positive leg
GP15_TD0N	1	I_A/O_A	1.0V	Port 15 pair 0 negative leg
GP15_TD1P	1	I_A/O_A	1.0V	Port 15 pair 1 positive leg
GP15_TD1N	1	I_A/O_A	1.0V	Port 15 pair 1 negative leg
GP15_TD2P	1	I_A/O_A	1.0V	Port 15 pair 2 positive leg
GP15_TD2N	1	I_A/O_A	1.0V	Port 15 pair 2 negative leg
GP15_TD3P	1	I_A/O_A	1.0V	Port 15 pair 3 positive leg
GP15_TD3N	1	I_A/O_A	1.0V	Port 15 pair 3 negative leg
DDR2/DDR3 Interface				
IP_DDR_AD[15:0]	16	O	1.8V/ 1.5V	DDR2/DDR3 address bus
IP_DDR_CS0_L	1	O	1.8V/ 1.5V	DDR2/DDR3 chip select 0
IP_DDR_CS1_L	1	O	1.8V/ 1.5V	DDR2/DDR3 chip select 1
IP_DDR_ODT	1	O	1.8V/ 1.5V	DDR2/DDR3 on-die termination enable
IP_DDR_BA0	1	O	1.8V/ 1.5V	DDR2/DDR3 bank address 0
IP_DDR_BA1	1	O	1.8V/ 1.5V	DDR2/DDR3 bank address 1
IP_DDR_BA2	1	O	1.8V/ 1.5V	DDR2/DDR3 bank address 2
IP_DDR_CAS_L	1	O	1.8V/ 1.5V	DDR2/DDR3 column address select
IP_DDR_CLK0_N	1	O	1.8V/ 1.5V	Negative leg of DDR2/DDR3 differential clock pair 0
IP_DDR_CLK0_P	1	O	1.8V/ 1.5V	Positive leg of DDR2/DDR3 differential clock pair 0
IP_DDR_CLK1_N	1	O	1.8V/ 1.5V	Negative leg of DDR2/DDR3 differential clock pair 1
IP_DDR_CLK1_P	1	O	1.8V/ 1.5V	Positive leg of DDR2/DDR3 differential clock pair 1
IP_DDR_CKE	1	O	1.8V/ 1.5V	DDR2/DDR3 clock enable
IP_DDR_DM0	1	O	1.8V/ 1.5V	DDR2/DDR3 data mask for byte lane 0
IP_DDR_DM1	1	O	1.8V/ 1.5V	DDR2/DDR3 data mask for byte lane 1
IP_DDR_DQ[15:0]	16	I/O	1.8V/ 1.5V	DDR2/DDR3 data bus
IP_DDR_DQS0_N	1	I/O	1.8V/ 1.5V	Negative leg of DDR2/DDR3 differential pair data strobe for byte lane 0.

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	Quantity	I/O	V	Pin Description
IP_DDR_DQS0_P	1	I/O	1.8V/ 1.5V	Positive leg of DDR2/DDR3 differential pair data strobe for byte lane 0.
IP_DDR_DQS1_N	1	I/O	1.8V/ 1.5V	Negative leg of DDR2/DDR3 differential pair data strobe for byte lane 1.
IP_DDR_DQS1_P	1	I/O	1.8V/ 1.5V	Positive leg of DDR2/DDR3 differential pair data strobe for byte lane 1.
IP_DDR_RAS_L	1	O	1.8V/ 1.5V	DDR2/DDR3 row address select.
IP_DDR_RST_L	1	O	1.5V	DDR2/DDR3 reset output.
IP_DDR_WE_L	1	O	1.8V/ 1.5V	DDR2/DDR3 write enable.
IP_DDR_ZQ	1	I/O	1.8V/ 1.5V	Output impedance calibration. This pin should be attached to a 240Ω 1% resister to GND (ground) for impedance calibration.
IP_DDR_VREF	1	O	0.9V/ 0.75V	0.9V (DDR_OVDD divided by two) DDR2 reference/ 0.75V(DDR_OVDD divided by two) DDR3 reference
Warpcore Signals				
WC0_RD[3:0]N	4	I	1.0V	Warpcore port 0 received serial data—Negative leg of the differential pair.
WC0_RD[3:0]P	4	I	1.0V	Warpcore port 0 received serial data—Positive leg of the differential pair.
WC0_REFCLKN	1	I	1.0V	Negative leg of Reference Clock In.
WC0_REFCLKP	1	I	1.0V	Positive leg of Reference Clock In.
WC0_TD[3:0]N	4	O	1.0V	Warpcore port 0 transmit serial data—Negative leg of the differential pair.
WC0_TD[3:0]P	4	O	1.0V	Warpcore port 0 transmit serial data—Positive leg of the differential pair.
WC1_RD[3:0]N	4	I	1.0V	Warpcore port 1 received serial data—Negative leg of the differential pair.
WC1_RD[3:0]P	4	I	1.0V	Warpcore port 1 received serial data—Positive leg of the differential pair.
WC1_REFCLKN	1	I	1.0V	Negative leg of Reference Clock In.
WC1_REFCLKP	1	I	1.0V	Positive leg of Reference Clock In.
WC1_TD[3:0]N	4	O	1.0V	Warpcore port 1 transmit serial data—Negative leg of the differential pair.
WC1_TD[3:0]P	4	O	1.0V	Warpcore port 1 transmit serial data—Positive leg of the differential pair.
QSGMII Port Signals				
QS2_RD[1:0]N	2	I	1.0V	QSGMII 2 received serial 5.0 Gbps data—Negative leg of the differential pair.
QS2_RD[1:0]P	2	I	1.0V	QSGMII 2 received serial 5.0 Gbps data—Positive leg of the differential pair.
QS2_TD[1:0]N	2	O	1.0V	QSGMII 2 transmit serial 5.0 Gbps data—Negative leg of the differential pair.

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	*Quantity*	*I/O*	*V*	*Pin Description*
QS2_TD[1:0]P	2	O	1.0V	QSGMII 2 transmit serial 5.0 Gbps data—Positive leg of the differential pair.
EXT_QS2_CLKP	1	O		Positive leg of differential reference clock out for external PHY.
EXT_QS2_CLKN	1	O		Negative leg of differential reference clock out for external PHY.
MII Port Signals				
RXC	1	I	3.3V	Receive Clock. 2.5/25 MHz input. This clock is recovered from the incoming analog waveforms and is used to synchronize the receive data: • In 100BASE-TX mode, the clock is 25 MHz, nibble-aligned on RXD[3:0]. • In 10BASE-T mode, the clock is 2.5 MHz, nibble-aligned on RXD[3:0]. Shared with LED_P0_2, GPIO8
TXC	1	I	3.3V	MII Transmit Clock This clock is used to synchronize the transmit data in MII mode. This clock input is 25 MHz in 100BASE-TX mode and 2.5 MHz in 10BASE-T mode. Shared with LED_P1_2, GPIO9.
RXD[3:0]	4	I	3.3V	Receive Data Input In 10BASE-T and 100BASE-TX mode, nibble-wide receive data is active on RXD[3:0] synchronous to TXC. RXD3 is the most significant bit. RXD3 shared with LED_P5_2, GPIO13 RXD2 shared with LED_P4_2, GPIO12 RXD1 shared with LED_P3_2, GPIO11 RXD0 shared with LED_P2_2, GPIO10
RXDV	1	I	3.3V	Receive Data Valid Active high. RXDV indicates that a receive frame is in progress and the data present on the RXD input pins are valid. Shared with LED_P6_2, GPIO14.
RXER	1	I	3.3V	Receive Error Detected Active high. Indicates that there has been an error during a receive frame. An illegal code or some other coding violation has been detected in the data received from the twisted-pair medium when both RXDV and RXER are high. Shared with LED_P7_2, GPIO15.
CRS	1	I	3.3V	Carrier Sense. Active-high. Indicates traffic on link. Shared with LED_P8_2, SCK

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	*Quantity*	*I/O*	*V*	*Pin Description*
COL	1	I	3.3V	Collision Detected. In half-duplex mode, active-high input indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous input signal. Shared with LED_P9_2, MISO.
TXD[3:0]	4	O	3.3V	Transmit Data Output. In 10BASE-T and 100BASE-TX mode, nibble-wide transmit data is output on TXD[3:0] synchronously TXD3 shared with LED_P13_2 TXD2 shared with LED_P12_2 TXD1 shared with LED_P11_2, SS_L TXD0 shared with LED_P10_2, MOSI
TXEN	1	O	3.3V	Transmit Enable. When TXEN is asserted, data on the TXD pins is encoded and transmitted. Shared with LED_P14_2.
TXER	1	O	3.3V	Transmit Error Asserted while TXER is active to force a bad code into the transmit data stream. Shared with LED_P15_2.
MIIM Interface				
IP_MDC	1	B_{PU}	3.3V	Serial management clock. Clause 22 compliant.
IP_MDIO	1	B_{PU}	3.3V	Serial management data. Clause 22 compliant.
GIG_MDC	1	B_{PU}	3.3V	Serial management clock, used to communicate to external GPHY devices under software control. Clause 22 compliant.
GIG_MDIO	1	B_{PU}	3.3V	Serial management data, used to communicate to external GPHY devices under software control. Clause 22 compliant.
XG_MDC	1	B_{PU}	3.3V/ 2.5V/ 1.2V	Serial management clock, used to communicate to external GPHY devices under software control. Clauses 22 and 45 compliant.
XG_MDIO	1	B_{PU}	3.3V/ 2.5V/ 1.2V	Serial management data, used to communicate to external GPHY devices under software control. Clauses 22 and 45 compliant.
Note: The voltage level of the XG MIIM Interface is determined by XG_VDDO.				
BSC Interface				
BSC_SA[1:0]	2	I_{PD}	3.3V	BSC Address [1:0]. • 0: Address is 0x80 (Default) • 1: Address is 0x81 • 2: Address is 0x82 • 3: Address is 0x83
BSC_SCL	1	B_{OD}	3.3V	BSC master clock. External pull-up resistor is required.

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	*Quantity*	*I/O*	*V*	*Pin Description*
BSC_SDA	1	B_{OD}	3.3V	BSC serial data. External pull-up resistor is required.
BroadSync Interface				
BS0_TIME_VAL	1	B	3.3V	BroadSync synchronized time value.
BS1_TIME_VAL	1	B	3.3V	Serially shifts the time value, one bit per rising edge of the BS_BIT_CLK. This signal can be configured through CMIC register as an output or an input. When it is configured as an output, the BS_TIME_VAL signal is driven off the rising edge of the BS_BIT_CLK. When it is configured as an input, BS_TIME_VAL signal is sampled off the negative edge of the BS_BIT_CLK.
BS0_SYNC	1	B	3.3V	BroadSync heartbeat clock that signal the start of the transmission of the synchronized time value. This signal can be configured through CMIC register as an output or an input. When it is configured as an output, the BS_SYNC signal is driven off the rising edge of the BS_BIT_CLK. When it is configured as an input, the BS_SYNC signal is sampled off the negative edge of the BS_BIT_CLK.
BS1_SYNC	1	B	3.3V	
BS0_BIT_CLK	1	B	3.3V	BroadSync bit clock.
BS1_BIT_CLK	1	B	3.3V	Used for the data transfer of the synchronized time value. When configured as outputs, the BS_SYNC and BS_TIME_VAL signals are driven off the rising edge of the BS_BIT_CLK. When configured as inputs, the BS_SYNC and BS_TIME_VAL signals are sampled off the negative edge of the BS_BIT_CLK.
TS_GPIO0	1	I_{PU}/ O_{PU}	3.3V	BroadSync GPIO bit 0 ***Note:*** This pin can be reset by resetting SYS_RST_L.
TS_GPIO1	1	I_{PU}/ O_{PU}	3.3V	BroadSync GPIO bit 1 ***Note:*** This pin can be reset by resetting SYS_RST_L.
BS0_PLL_CLKN	1	O	1.0V	BroadSync PLL test clock differential output. Used during manufacturing test only. Should be 'No Connect' for normal operation.
BS0_PLL_CLKP	1	O	1.0V	
BS1_PLL_CLKN	1	O	1.0V	
BS1_PLL_CLKP	1	O	1.0V	
BS0_PLL_REFCLKN	1	I	1.0V	Broadsync 0 PLL external reference clock inputs for BroadSync applications.
BS0_PLL_REFCLKP	1	I	1.0V	
BS1_PLL_REFCLKN	1	I	1.0V	Broadsync 1 PLL external reference clock inputs for BroadSync applications.
BS1_PLL_REFCLKP	1	I	1.0V	
Synchronous Ethernet Interface				

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	Quantity	I/O	V	Pin Description
EXT_RCVRD_CLK0	1	I_{PD}	3.3V	External Clock Inputs These are inputs for recovered clocks from external sources.
EXT_RCVRD_CLK0_VLD	1	I_{PD}	3.3V	
EXT_RCVRD_CLK1	1	I_{PD}	3.3V	
EXT_RCVRD_CLK1_VLD	1	I_{PD}	3.3V	
L1_RCVRD_CLK	1	O	3.3V	Primary recovered clock. Recovered clock from one of the ports of the device. This clock is sent out to support L1 synchronization.
L1_RCVRD_CLK_VALID	1	O	3.3V	Indicates the primary recovered clock is valid Link status needed for the recovered clock. When this signal is set to 1, L1_RCVRD_CLK is generated based on the recovered clock.
L1_RCVRD_CLK_BKUP	1	O	3.3V	Secondary recovered clock. Backup recovered clock from one of the ports of the device. This clock is used when the primary recovered clock is not reliable.
L1_RCVRD_CLK_VALID_BKUP	1	O	3.3V	Indicates the secondary recovered clock is valid Link status needed for the recovered clock. When this signal is set to 1, L1_RCVRD_CLK_BKUP is generated based on the recovered clock.
1588 Interface				
TS_PLL_REFCLKN	1	I	1.0V	Time stamp PLL external reference clock
TS_PLL_REFCLKP	1	I	1.0V	Time stamp PLL external reference clock
Miscellaneous Signals				
SYS_RST_L	1	I_{PU}	3.3V	Reset input for the whole chip
RDAC[3:0]	4	I_B/O_B	–	DAC Bias Resistor. Adjusts the drive level of the transmit DAC. A 6.04 K ±1% resistor to GND is required.
VSS_SENSE	1	O	0V	Ground monitor. Required for remote sensing of GND rail. This pin connects directly to die GND rail.
VDD_SENSE	1	O	1.0V	Core voltage monitor. Required for remote sensing of VDDC rail. This pin connects directly to die VDDC rail.
AVS0	1	O	3.3V	Reserved
LOS_0	1	I_{PD}	3.3V	Warpcore Lost of Signal (LOS) interface It is programmable to select either WC0 or WC1 to be connected to LOS inputs. Refer to the Broadcom SDK for details.
LOS_1	1	I_{PD}	3.3V	
LOS_2	1	I_{PD}	3.3V	
LOS_3	1	I_{PD}	3.3V	
DNC	29	–	–	Do not connect these pins.
Miscellaneous PLL Signals				

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	Quantity	I/O	V	Pin Description
XG_PLL2_REFCLKN	1	I	1.0V	PCIE and DDR REFCLK PLL external reference clock input.
XG_PLL2_REFCLKP	1	I	1.0V	
LC_PLL1_REFCLKN	1	I	1.0V	Warpcore REFCLK PLL external reference clock input.
LC_PLL1_REFCLKP	1	I	1.0V	
LC_PLL0_REFCLKN	1	I	1.0V	QSGMII/QGPHYREFCLK PLL external reference clock input.
LC_PLL0_REFCLKP	1	I	1.0V	
DIGITAL POWER				
IP_DDR_VDDO	–	PWR	1.8V/ 1.5V	IP_DDR Power • DDR3 (1.5V) • DDR2 (1.8V)
PCIE_VDD	–	PWR	1.0V	Power for PCIe
PCIE_PVDD	1	PWR	1.0V	1.0V, Filtered PLL voltage for PCIe clock distribution.
QS2_VDD	–	PWR	1.0V	Power for QSGMII 2
VDDC	–	PWR	1.0V	Power for core
VDD33	–	PWR	3.3V	3.3V VDD
IP_PFLASH_VDDO	–	PWR	3.3V	Power for PFLASH
XG_VDDO	1	PWR	3.3V/ 2.5V/ 1.2V	Power for MIIM_XG interface • 1.2V for Clause 45 compliant • 2.5V or 3.3V for Clause 22 compliant
IP_DDR_VDDO_CLK	1	PWR	1.8V/ 1.5V	Power supply for DDR2/3 clock I/O. Same voltage level as IP_DDR_VDDO, need LC filter so that it is not affected by SSO noise from the main IP_DDR_VDDO supply.
CORE_PLL_VDD33	1	PWR	3.3V	Power for core PLL.
TS_PLL_VDD33	1	PWR	3.3V	Power for time sync PLL.
GEN_PLL_VDD10	1	PWR	1.0V	Power for generic PLL.
GP0_PLLVDD10	1	PWR	1.0V	1.0V for QGPHY 0 PLL.
GP0_PLLVDD33	1	PWR	3.3V	3.3V for QGPHY 0 PLL, should be connected to GP0_BVDD33 on PCB.
GP1_PLLVDD10	1	PWR	1.0V	1.0V for QGPHY 1 PLL
GP1_PLLVDD33	1	PWR	3.3V	3.3V for QGPHY 1 PLL, should be connected to GP1_BVDD33 on PCB.
GP2_PLLVDD10	1	PWR	1.0V	1.0V for QGPHY 2 PLL
GP2_PLLVDD33	1	PWR	3.3V	3.3V for QGPHY 2 PLL, should be connected to GP2_BVDD33 on PCB.
GP3_PLLVDD10	1	PWR	1.0V	1.0V for QGPHY 3 PLL
GP3_PLLVDD33	1	PWR	3.3V	3.3V for QGPHY 3 PLL, should be connected to GP3_BVDD33 on PCB.
ANALOG POWER				
GP_AVDDL	–	PWR	1.0V	1.0V for QGPHY analog supply
GP_AVDDH	–	PWR	3.3V	3.3V for QGPHY analog supply

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	Quantity	I/O	V	Pin Description
LC_PLL0_AVDD33	1	PWR	3.3V	QGPHY and QSGMII PLL
LC_PLL1_AVDD33	1	PWR	3.3V	Warpcore PLL
BS0_PLL_AVDD33	1	PWR	3.3V	BroadSync 0 PLL Power.
BS1_PLL_AVDD33	1	PWR	3.3V	BroadSync 1 PLL Power.
XG_PLL2_AVDD33	1	PWR	3.3V	PCIe PLL
GP0_BVDD33	1	PWR	3.3V	3.3V for QGPHY 0 Bandgap, should be connected to GP0_PLLVDD33 on PCB.
GP1_BVDD33	1	PWR	3.3V	3.3V for QGPHY 1 Bandgap, should be connected to GP1_PLLVDD33 on PCB.
GP2_BVDD33	1	PWR	3.3V	3.3V for QGPHY 2 Bandgap, should be connected to GP2_PLLVDD33 on PCB.
GP3_BVDD33	1	PWR	3.3V	3.3V for QGPHY 3 Bandgap, should be connected to GP3_PLLVDD33 on PCB.
IP_DDR_AVDD	1	PWR	1.5V/ 1.8V	IP_DDR PHY PLL • DDR3 (1.5V) • DDR2 (1.8V)
WC0_TVDD10	–	PWR	1.0V	1.0V, Filtered WC0 transmit power.
WC0_RVDD10	–	PWR	1.0V	1.0V, Filtered WC0 received power.
WC0_PVDD10	1	PWR	1.0V	1.0V, Filtered PLL voltage for WC0 clock distribution.
WC1_TVDD10	–	PWR	1.0V	1.0V, Filtered WC1 transmit power.
WC1_RVDD10	–	PWR	1.0V	1.0V, Filtered WC1 received power.
WC1_PVDD10	–	PWR	1.0V	1.0V, Filtered PLL voltage for WC1 clock distribution.
QS2_PVDD	–	PWR	1.0V	1.0V, Filtered PLL voltage for QSGMII 2 clock distribution.
AVDD33	1	PWR	3.3V	Analog Power for PVT Monitor.
XTAL_AVDD	1	PWR	1.0V	Power for internal oscillator.
GROUND				
GND	–	GND	0V	Ground
GEN_PLL_VSS	1	GND	0V	Ground
ANALOG GROUND				
AVSS	–	GND	0V	Ground
BS0_PLL_AVSS	–	GND	0V	Ground
BS1_PLL_AVSS	–	GND	0V	Ground
CORE_PLL_AVSS	–	GND	0V	Ground
LC_PLL0_AVSS	–	GND	0V	Ground
LC_PLL1_AVSS	–	GND	0V	Ground
PCIE_AVSS	–	GND	0V	Ground
QS2_AVSS	–	GND	0V	Ground
TS_PLL_AVSS	–	GND	0V	Ground
WC_AVSS	–	GND	0V	Ground

Table 15: BCM56150 Hardware Signals (Cont.)

Pin Names	*Quantity*	*I/O*	*V*	*Pin Description*
XG_PLL2_AVSS	–	GND	0V	Ground
XTAL_AVSS	–	GND	0V	Ground

Pin List by Pin Name

Table 16: Pin List by Pin Name - BCM56150 Devices

Ball	Signal Name
A10	GND
A11	IP_DDR_DQ4
A12	IP_DDR_VREF
A13	GND
A14	IP_DDR_VDDO
A15	IP_DDR_BA2
A16	IP_DDR_AD3
A17	IP_DDR_AD7
A18	IP_DDR_VDDO
A2	GND
A20	IP_DDR_CLK1_P
A21	IP_DDR_CS1_L
A22	GND
A23	WC_AVSS
A24	WC1_TD0P
A25	WC_AVSS
A26	WC1_TD1N
A27	WC_AVSS
A28	WC1_TD2P
A29	WC_AVSS
A3	IP_DDR_DM0
A30	WC1_TD3P
A31	WC_AVSS
A32	WC0_REFCLKP
A33	WC0_REFCLKN
A34	WC_AVSS
A4	IP_DDR_DQ10
A6	IP_DDR_VDDO
A7	IP_DDR_DQ14
A8	IP_DDR_DQ15
AA1	UART1_RI_L
AA12	PCIE_VDD
AA13	PCIE_AVSS
AA14	GND
AA15	GND
AA16	VDDC
AA17	VDDC
AA18	VDDC
AA19	VDDC
AA2	UART1_DTR_L
AA20	VDDC
AA21	VDDC
AA22	VDDC
AA23	VDDC
AA24	VDDC
AA28	GND
AA29	DNC
AA3	UART1_DCD_L
AA30	DNC
AA31	GND
AA32	GND
AA33	DNC
AA34	XTAL_AVSS
AA35	XTAL_AVSS
AA4	GND
AA5	PCIE_AVSS
AA6	PCIE_CLKOUTP
AA7	PCIE_CLKOUTN
AA8	PCIE_AVSS
AB1	UART1_RTS_L/ SFLASH_BYTE_ ADDR
AB12	PCIE_VDD
AB13	PCIE_AVSS
AB14	GND
AB15	GND
AB16	GND
AB17	GND
AB18	GND
AB19	GND
AB2	UART1_CTS_L
AB20	GND
AB21	GND
AB22	GND
AB23	GND
AB24	GND
AB28	LC_PLL1_AVDD33
AB29	LC_PLL1_AVSS
AB3	UART1_DSR_L
AB30	LC_PLL1_REFCLKP
AB31	LC_PLL1_REFCLKN
AB32	LC_PLL1_AVSS
AB33	XTAL_AVDD
AB34	XTALN
AB35	XTALP
AB4	GND
AB5	PCIE_AVSS
AB6	PCIE_TDN
AB7	PCIE_TDP
AB8	PCIE_AVSS
AC12	AVSS
AC13	AVSS
AC14	AVSS
AC15	AVSS
AC16	AVSS
AC17	AVSS
AC18	AVSS
AC19	AVSS
AC2	UART1_TX
AC20	AVSS
AC21	AVSS
AC22	AVSS
AC23	AVSS
AC24	AVSS
AC28	LC_PLL1_AVSS
AC29	LC_PLL1_AVSS
AC3	UART1_RX
AC30	LC_PLL0_AVSS
AC31	GND
AC32	GND
AC33	XTAL_AVSS
AC34	XTAL_AVSS
AC35	XTAL_AVSS
AC4	GND
AC5	XG_PLL2_AVSS
AC6	DNC
AC7	DNC
AC8	XG_PLL2_AVSS
AD1	UART2_RX
AD12	GP_AVDDL
AD13	GP_AVDDL
AD14	GP_AVDDL
AD15	GP_AVDDL
AD16	GP_AVDDL
AD17	GP_AVDDL
AD18	GP_AVDDL
AD19	GP_AVDDL
AD2	UART2_TX
AD20	GP_AVDDL
AD21	GP_AVDDL
AD22	GP_AVDDL
AD23	GP_AVDDL
AD24	GP_AVDDL
AD28	LC_PLL0_AVDD33
AD29	LC_PLL0_AVSS
AD3	LED_P1_1
AD30	LC_PLL0_REFCLKP

Ball	Signal Name
AD31	LC_PLL0_REFCLKN
AD32	LC_PLL0_AVSS
AD33	QS2_AVSS
AD34	QS2_TD0N
AD35	QS2_TD0P
AD4	LED_P1_0
AD5	LED_P2_0
AD6	GND
AD7	GND
AD8	VDD33
AE1	LED_P3_0
AE2	LED_P3_1
AE28	QS2_AVSS
AE29	QS2_AVSS
AE3	LED_P4_0
AE30	QS2_AVSS
AE31	QS2_AVSS
AE32	QS2_AVSS
AE33	QS2_AVSS
AE34	QS2_AVSS
AE35	QS2_AVSS
AE4	LED_P4_1
AE5	LED_P2_1
AE6	LED_P0_1
AE7	LED_P0_0
AE8	GND
AF2	LED_P5_0
AF28	QS2_PVDD
AF29	DNC
AF3	LED_P5_1
AF30	QS2_VDD
AF31	QS2_TD1N
AF32	QS2_TD1P
AF33	QS2_AVSS
AF34	QS2_RD0N
AF35	QS2_RD0P
AF4	GND
AF5	LED_P11_1
AF6	LED_P10_1
AF7	LED_P9_1
AF8	VDD33
AG1	LED_P6_1
AG2	LED_P6_0
AG28	QS2_PVDD
AG29	DNC
AG3	LED_P14_0
AG30	QS2_VDD
AG31	QS2_AVSS
AG32	QS2_AVSS
AG33	QS2_AVSS
AG34	QS2_AVSS
AG35	QS2_AVSS
AG4	LED_P13_1
AG5	LED_P12_1
AG6	LED_P11_0
AG7	LED_P10_0
AG8	GND
AH1	LED_P7_1
AH10	GP_AVDDH
AH11	GP_AVDDH
AH12	GP_AVDDH
AH13	AVSS
AH14	AVSS
AH15	GP0_PLLVDD10
AH16	AVSS
AH17	GP1_PLLVDD10
AH18	AVSS
AH19	GP2_PLLVDD10
AH2	LED_P7_0
AH20	AVSS
AH21	GP3_PLLVDD10
AH22	AVSS
AH23	AVSS
AH24	GP_AVDDH
AH25	GP_AVDDH
AH26	GP_AVDDH
AH27	AVSS
AH28	QS2_AVSS
AH29	QS2_VDD
AH3	GP0_TD0N
AH30	QS2_VDD
AH31	QS2_RD1P
AH32	QS2_RD1N
AH33	QS2_AVSS
AH34	EXT_QS2_CLKN
AH35	EXT_QS2_CLKP
AH4	GP0_TD0P
AH5	LED_P13_0
AH6	LED_P12_0
AH7	LED_P9_0
AH8	LED_P8_0
AH9	AVSS
AJ10	GP_AVDDH
AJ11	GP_AVDDH
AJ12	AVSS
AJ13	GP0_BVDD33
AJ14	AVSS
AJ15	GP0_PLLVDD33
AJ16	AVSS
AJ17	GP1_PLLVDD33
AJ18	AVSS
AJ19	GP2_PLLVDD33
AJ2	GP0_TD1N
AJ20	AVSS
AJ21	GP3_PLLVDD33
AJ22	AVSS
AJ23	GP2_BVDD33
AJ24	AVSS
AJ25	GP_AVDDH
AJ26	GP_AVDDH
AJ27	GP_AVDDH
AJ28	AVSS
AJ29	QS2_AVSS
AJ3	GP0_TD1P
AJ30	QS2_AVSS
AJ31	QS2_AVSS
AJ32	QS2_AVSS
AJ33	QS2_AVSS
AJ34	LC_PLL0_AVSS
AJ35	LC_PLL0_AVSS
AJ4	AVSS
AJ5	GND
AJ6	LED_P14_1
AJ7	LED_P8_1
AJ8	AVSS
AJ9	GP_AVDDH
AK1	GP0_TD2P
AK10	AVSS
AK11	AVSS
AK12	AVSS
AK13	GP1_BVDD33
AK14	AVSS
AK15	AVSS
AK16	AVSS
AK17	AVSS
AK18	AVSS
AK19	AVSS
AK2	GP0_TD2N
AK20	AVSS
AK21	AVSS
AK22	AVSS
AK23	GP3_BVDD33
AK24	AVSS
AK25	AVSS
AK26	AVSS
AK27	AVSS
AK28	AVSS
AK29	AVSS
AK3	GP0_TD3N

Ball	Signal Name
AK30	AVSS
AK31	AVSS
AK32	AVSS
AK33	GP15_TD0P
AK34	GP15_TD0N
AK4	GP0_TD3P
AK5	AVSS
AK6	LED_P15_1
AK7	LED_P15_0
AK8	AVSS
AK9	AVSS
AL1	GP1_TD3N
AL10	AVSS
AL11	AVSS
AL12	RDAC0
AL13	AVSS
AL14	AVSS
AL15	RDAC1
AL16	AVSS
AL17	GP_AVDDH
AL18	GP_AVDDH
AL19	GP_AVDDH
AL2	GP1_TD3P
AL20	AVSS
AL21	RDAC2
AL22	AVSS
AL23	AVSS
AL24	RDAC3
AL25	AVSS
AL26	AVSS
AL27	DNC
AL28	AVSS
AL29	AVSS
AL3	GP1_TD2N
AL30	DNC
AL31	AVSS
AL32	GP15_TD1P
AL33	GP15_TD1N
AL34	GP15_TD2P
AL35	GP15_TD2N
AL4	GP1_TD2P
AL5	AVSS
AL6	DNC
AL7	AVSS
AL8	AVSS
AL9	DNC
AM10	GP5_TD3P
AM11	GP5_TD1P
AM12	AVSS
AM13	GP6_TD1P
AM14	GP6_TD3P
AM15	AVSS
AM16	GP7_TD1P
AM17	GP8_TD0P
AM18	AVSS
AM19	GP8_TD3P
AM2	GP1_TD1N
AM20	GP9_TD2P
AM21	AVSS
AM22	GP10_TD0P
AM23	GP10_TD2P
AM24	AVSS
AM25	GP11_TD2P
AM26	GP11_TD0P
AM27	AVSS
AM28	GP12_TD2P
AM29	GP13_TD3P
AM3	GP1_TD1P
AM30	AVSS
AM31	GP13_TD0P
AM32	GP14_TD1P
AM33	AVSS
AM34	GP15_TD3P
AM35	GP15_TD3N
AM4	AVSS
AM5	GP3_TD3P
AM6	AVSS
AM7	GP3_TD0P
AM8	GP4_TD1P
AM9	AVSS
AN1	GP1_TD0P
AN10	GP5_TD3N
AN11	GP5_TD1N
AN12	GP5_TD0P
AN13	GP6_TD1N
AN14	GP6_TD3N
AN15	GP7_TD3P
AN16	GP7_TD1N
AN17	GP8_TD0N
AN18	GP8_TD1P
AN19	GP8_TD3N
AN2	GP1_TD0N
AN20	GP9_TD2N
AN21	GP9_TD1P
AN22	GP10_TD0N
AN23	GP10_TD2N
AN24	GP10_TD3P
AN25	GP11_TD2N
AN26	GP11_TD0N
AN27	GP12_TD0P
AN28	GP12_TD2N
AN29	GP13_TD3N
AN3	GP2_TD0N
AN30	GP13_TD2P
AN31	GP13_TD0N
AN32	GP14_TD1N
AN33	GP14_TD2P
AN34	GP14_TD3P
AN35	GP14_TD3N
AN4	GP2_TD0P
AN5	GP3_TD3N
AN6	GP3_TD2P
AN7	GP3_TD0N
AN8	GP4_TD1N
AN9	GP4_TD2P
AP1	AVSS
AP10	GP4_TD3N
AP11	GP5_TD2P
AP12	GP5_TD0N
AP13	GP6_TD0N
AP14	GP6_TD2P
AP15	GP7_TD3N
AP16	GP7_TD2N
AP17	GP7_TD0P
AP18	GP8_TD1N
AP19	GP8_TD2N
AP2	AVSS
AP20	GP9_TD3P
AP21	GP9_TD1N
AP22	GP9_TD0N
AP23	GP10_TD1P
AP24	GP10_TD3N
AP25	GP11_TD3N
AP26	GP11_TD1P
AP27	GP12_TD0N
AP28	GP12_TD1N
AP29	GP12_TD3P

Ball	Signal Name
AP3	GP2_TD1P
AP30	GP13_TD2N
AP31	GP13_TD1N
AP32	GP14_TD0P
AP33	GP14_TD2N
AP34	AVSS
AP35	AVSS
AP4	GP2_TD2P
AP5	GP2_TD3P
AP6	GP3_TD2N
AP7	GP3_TD1N
AP8	GP4_TD0P
AP9	GP4_TD2N
AR10	GP4_TD3P
AR11	GP5_TD2N
AR13	GP6_TD0P
AR14	GP6_TD2N
AR16	GP7_TD2P
AR17	GP7_TD0N
AR19	GP8_TD2P
AR2	AVSS
AR20	GP9_TD3N
AR22	GP9_TD0P
AR23	GP10_TD1N
AR25	GP11_TD3P
AR26	GP11_TD1N
AR28	GP12_TD1P
AR29	GP12_TD3N
AR3	GP2_TD1N
AR31	GP13_TD1P
AR32	GP14_TD0N
AR34	AVSS
AR4	GP2_TD2N
AR5	GP2_TD3N
AR7	GP3_TD1P
AR8	GP4_TD0N
B1	IP_DDR_VDDO
B10	IP_DDR_DQS0_P
B11	IP_DDR_VDDO
B12	IP_DDR_DQ5
B13	IP_DDR_RAS_L
B14	IP_DDR_CS0_L
B15	GND
B16	IP_DDR_AD0
B17	GND
B18	IP_DDR_AD2
B19	IP_DDR_AD13
B2	GND
B20	IP_DDR_CLK1_N
B21	IP_DDR_VDDO
B22	DNC
B23	WC_AVSS
B24	WC1_TD0N
B25	WC_AVSS
B26	WC1_TD1P
B27	WC_AVSS
B28	WC1_TD2N
B29	WC_AVSS
B3	IP_DDR_VDDO
B30	WC1_TD3N
B31	WC_AVSS
B32	WC_AVSS
B33	WC_AVSS
B34	WC_AVSS
B35	WC_AVSS
B4	IP_DDR_DQ8
B5	IP_DDR_DQ11
B6	IP_DDR_DQS1_P
B7	GND
B8	IP_DDR_DQ13
B9	IP_DDR_DM1
C1	IP_DDR_DQ3
C10	IP_DDR_DQ2
C11	IP_DDR_DQS0_N
C12	GND
C13	IP_DDR_CAS_L
C14	IP_DDR_WE_L
C15	IP_DDR_BA0
C16	IP_DDR_VDDO
C17	IP_DDR_AD5
C18	IP_DDR_RST_L
C19	IP_DDR_AD9
C2	IP_DDR_DQ1
C20	GND
C21	IP_DDR_ZQ
C22	DNC
C23	WC_AVSS
C24	WC_AVSS
C25	WC_AVSS
C26	WC_AVSS
C27	WC_AVSS
C28	WC_AVSS
C29	WC_AVSS
C3	IP_DDR_DQ7
C30	WC_AVSS
C31	WC_AVSS
C32	DNC
C33	WC_AVSS
C34	WC0_TD3N
C35	WC0_TD3P
C4	GND
C5	IP_DDR_DQ9
C6	IP_DDR_DQS1_N
C7	IP_DDR_DQ12
C8	IP_DDR_VDDO
C9	IP_DDR_DQ6
D1	GND
D10	IP_DDR_VDDO
D11	GND
D12	IP_DDR_VDDO_CLK
D13	IP_DDR_VDDO
D14	GND
D15	IP_DDR_AVDD
D16	GND
D17	IP_DDR_VDDO
D18	GND
D19	IP_DDR_VDDO
D2	IP_DDR_CLK0_P
D20	IP_MDIO
D21	JTDO
D22	WC_AVSS
D23	WC_AVSS
D24	WC_AVSS
D25	WC_AVSS
D26	WC_AVSS
D27	WC_AVSS
D28	WC_AVSS
D29	WC_AVSS
D3	IP_DDR_DQ0
D30	WC_AVSS
D31	WC_AVSS
D32	DNC
D33	WC_AVSS
D34	WC_AVSS
D35	WC_AVSS
D4	GND
D5	IP_DDR_VDDO
D6	GND
D7	IP_DDR_VDDO
D8	GND
D9	GND
E1	IP_DDR_CKE
E10	L1_RCVRD_CLK_VALID
E11	L1_RCVRD_CLK_VALID_BKUP
E12	GND
E13	GPIO0
E14	GPIO1
E15	GND
E16	IP_BOOT_DEV0
E17	IP_BOOT_DEV1
E18	IP_BOOT_DEV2
E19	IP_MDC
E2	IP_DDR_VDDO

Ball	Signal Name
E20	JTDI
E21	JTCK
E22	WC_AVSS
E23	WC1_RD3N
E24	WC_AVSS
E25	WC1_RD2N
E26	WC_AVSS
E27	WC1_RD1N
E28	WC_AVSS
E29	WC1_RD0N
E3	IP_DDR_CLK0_N
E30	WC_AVSS
E31	WC0_RD0N
E32	WC_AVSS
E33	WC_AVSS
E34	WC0_TD2N
E35	WC0_TD2P
E4	IP_DDR_ODT
E5	BS1_BIT_CLK
E6	BS1_TIME_VAL
E7	EXT_UC_PRESENT
E8	BS0_TIME_VAL
E9	L1_RCVRD_CLK
F1	IP_DDR_BA1
F10	EXT_RCVRD_CLK0_VLD
F11	EXT_RCVRD_CLK1
F12	L1_RCVRD_CLK_BKUP
F13	GPIO2
F14	GPIO3
F15	GPIO4
F16	GPIO5
F17	GPIO6
F18	GPIO7
F19	JTMS
F2	IP_DDR_AD15
F20	BSC_SCL
F21	JTRST_L
F22	WC_AVSS
F23	WC1_RD3P
F24	WC_AVSS
F25	WC1_RD2P
F26	WC_AVSS
F27	WC1_RD1P
F28	WC_AVSS
F29	WC1_RD0P
F3	GND
F30	WC_AVSS
F31	WC0_RD0P
F32	WC_AVSS
F33	WC_AVSS
F34	WC_AVSS
F35	WC_AVSS
F4	GND
F5	DNC
F6	BS0_BIT_CLK
F7	BS0_SYNC
F8	BS1_SYNC
F9	EXT_RCVRD_CLK0
G10	PCIE_PME_WAKE_L
G11	TS_GPIO0
G12	TS_GPIO1
G13	PCIE_INTR_L
G14	LOS_0
G15	LOS_1
G16	LOS_2
G17	LOS_3
G18	GND
G19	JTCE1
G2	IP_DDR_AD12
G20	BSC_SDA
G21	JTCE
G22	WC1_REFCLKN
G23	WC_AVSS
G24	WC_AVSS
G25	WC_AVSS
G26	WC_AVSS
G27	WC_AVSS
G28	WC_AVSS
G29	WC_AVSS
G3	IP_DDR_AD10
G30	WC_AVSS
G31	WC_AVSS
G32	WC_AVSS
G33	WC_AVSS
G34	WC0_TD1N
G35	WC0_TD1P
G4	IP_DDR_VDDO
G5	LED_P3_2/RXD1/GPIO11
G6	LED_P2_2/RXD0/GPIO10
G7	LED_P1_2/TXC/GPIO9
G8	LED_P0_2/RXC/GPIO8
G9	EXT_RCVRD_CLK1_VLD
H1	IP_DDR_VDDO
H10	GND
H11	VDD33
H12	GND
H13	VDD33
H14	GND
H15	VDD33
H16	GND
H17	VDD33
H18	GND
H19	GND
H2	IP_DDR_AD6
H20	BSC_SA0
H21	BSC_SA1
H22	WC1_REFCLKP
H23	WC_AVSS
H24	WC_AVSS
H25	WC1_PVDD10
H26	WC1_PVDD10
H27	WC_AVSS
H28	WC_AVSS
H29	WC_AVSS
H3	IP_DDR_AD1
H30	WC0_RD1P
H31	WC0_RD1N
H32	WC_AVSS
H33	WC_AVSS
H34	WC_AVSS
H35	WC_AVSS
H4	IP_DDR_VDDO
H5	LED_P6_2/RXDV/GPIO14
H6	LED_P5_2/RXD3/GPIO13
H7	LED_P4_2/RXD2/GPIO12
H8	GND
H9	GND
J1	IP_DDR_AD8
J2	GND
J28	WC_AVSS
J29	WC_AVSS
J3	IP_DDR_AD4
J30	WC_AVSS
J31	WC_AVSS
J32	WC_AVSS
J33	WC_AVSS
J34	WC0_TD0P
J35	WC0_TD0N
J4	GND
J5	LED_P9_2/COL/MISO
J6	LED_P8_2/CRS/SCK
J7	LED_P7_2/RXER/GPIO15
J8	PCIE_PERST_L
K1	IP_DDR_AD14

Ball	Signal Name
K2	IP_DDR_VDDO
K28	WC0_PVDD10
K29	WC_AVSS
K3	IP_DDR_AD11
K30	WC0_RD2P
K31	WC0_RD2N
K32	WC_AVSS
K33	WC_AVSS
K34	WC_AVSS
K35	WC_AVSS
K4	SYS_RST_L
K5	LED_P12_2/ TXD2
K6	LED_P11_2/ TXD1/SS_L
K7	LED_P10_2/ TXD0/MOSI
K8	GND
L1	GND
L2	XG_PLL2_AVSS
L28	WC0_PVDD10
L29	WC_AVSS
L3	XG_PLL2_AVSS
L30	WC_AVSS
L31	WC_AVSS
L32	WC_AVSS
L33	WC_AVSS
L34	WC_AVSS
L35	WC_AVSS
L4	GND
L5	LED_P15_2/ TXER
L6	LED_P14_2/ TXEN
L7	LED_P13_2/ TXD3
L8	VDD33
M1	XG_PLL2_REFCLKN
M12	AVDD33
M13	GND
M14	GND
M15	GND
M16	GND
M17	GND
M18	WC_AVSS
M19	WC1_TVDD10
M2	XG_PLL2_REFCLKP
M20	WC_AVSS
M21	WC1_RVDD10
M22	WC_AVSS
M23	WC0_RVDD10
M24	WC0_RVDD10
M28	WC_AVSS
M29	WC_AVSS
M3	XG_PLL2_AVDD33
M30	WC0_RD3P
M31	WC0_RD3N
M32	WC_AVSS
M33	WC_AVSS
M34	IP_PFLASH_CS1_L
M35	IP_PFLASH_WEN_L
M4	XG_PLL2_AVSS
M5	GND
M6	LED_DATA/ EXT_UC_IS_SPI
M7	LED_CLK
M8	GND
N1	DNC
N12	DNC
N13	DNC
N14	GND
N15	GND
N16	GND
N17	GND
N18	WC_AVSS
N19	WC1_TVDD10
N2	DNC
N20	WC_AVSS
N21	WC1_RVDD10
N22	WC_AVSS
N23	WC_AVSS
N24	WC_AVSS
N28	WC_AVSS
N29	WC_AVSS
N3	CORE_PLL_AVSS
N30	WC_AVSS
N31	WC_AVSS
N32	WC_AVSS
N33	GND
N34	IP_PFLASH_AD15/CLE
N35	IP_PFLASH_AD14/ALE
N4	AVS0
N5	GND
N6	SFLASH_CS_L
N7	SFLASH_IO1
N8	VDD33
P1	BS1_PLL_REFCLKN
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	WC_AVSS
P19	WC_AVSS
P2	BS1_PLL_REFCLKP
P20	WC_AVSS
P21	WC_AVSS
P22	WC_AVSS
P23	WC0_TVDD10
P24	WC0_TVDD10
P28	IP_PFLASH_RB_L
P29	GND
P3	BS1_PLL_AVSS
P30	OSC_XTAL_SEL
P31	GND
P32	GND
P33	IP_PFLASH_AD22
P34	IP_PFLASH_AD23
P4	GND
P5	GND
P6	SFLASH_IO0
P7	SFLASH_CLK
P8	GND
R1	BS1_PLL_CLKN
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND
R19	GND
R2	BS1_PLL_CLKP
R20	GND
R21	GND
R22	WC_AVSS
R23	WC_AVSS
R24	WC_AVSS
R28	IP_PFLASH_AD5/ PCIE_FORCE_GEN1
R29	IP_PFLASH_AD1/ WP_L
R3	BS1_PLL_AVSS
R30	IP_PFLASH_AD3/ PCIE_RC_MODE
R31	IP_PFLASH_AD2/ PCIE_IF_ENABLE

Ball	Signal Name
R32	IP_PFLASH_AD24/IP_DDR_TYPE
R33	IP_PFLASH_AD16
R34	IP_PFLASH_DATA15
R35	IP_PFLASH_DATA7
R4	BS1_PLL_AVDD33
R5	GND
R6	SFLASH_IO2
R7	SFLASH_IO3
R8	VDD33
T1	BS0_PLL_CLKN
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	VSS_SENSE
T18	VDD_SENSE
T19	GND
T2	BS0_PLL_CLKP
T20	GND
T21	GND
T22	GND
T23	GND
T24	GND
T28	IP_PFLASH_VDDO
T29	IP_PFLASH_AD4/ PCIE_REFCLK_SEL
T3	BS0_PLL_AVSS
T30	IP_PFLASH_AD7/ NAND_TYPE1
T31	IP_PFLASH_AD17
T32	IP_PFLASH_DATA14
T33	IP_PFLASH_DATA6
T34	IP_PFLASH_DATA5
T35	IP_PFLASH_DATA13
T4	BS0_PLL_AVDD33
T5	GND
T6	XG_MDIO
T7	XG_MDC
T8	XG_VDDO
U1	BS0_PLL_REFCLKP
U12	GEN_PLL_VDD10
U13	GEN_PLL_VSS
U14	GND
U15	GND
U16	GND
U17	GND
U18	GND
U19	GND
U2	BS0_PLL_REFCLKN
U20	GND
U21	GND
U22	GND
U23	GND
U24	GND
U28	GND
U29	IP_PFLASH_AD18
U3	BS0_PLL_AVSS
U30	IP_PFLASH_AD6/ NAND_TYPE0
U31	IP_PFLASH_AD20/ NAND_DATA_WIDTH
U32	GND
U33	IP_PFLASH_DATA12
U34	IP_PFLASH_DATA4
U4	GND
U5	GND
U6	GIG_MDIO
U7	GIG_MDC
U8	GND
V1	DNC
V12	PCIE_AVSS
V13	PCIE_AVSS
V14	GND
V15	GND
V16	VDDC
V17	VDDC
V18	VDDC
V19	VDDC
V2	DNC
V20	VDDC
V21	VDDC
V22	VDDC
V23	VDDC
V24	VDDC
V28	IP_PFLASH_VDDO
V29	IP_PFLASH_AD9/ NAND_TYPE3
V3	TS_PLL_AVSS
V30	IP_PFLASH_AD19
V31	IP_PFLASH_AD21
V32	IP_PFLASH_DATA11
V33	IP_PFLASH_DATA3
V34	IP_PFLASH_DATA10
V35	IP_PFLASH_DATA2
V4	CORE_PLL_VDD33
V5	CORE_PLL_AVSS
V6	PCIE_AVSS
V7	PCIE_AVSS
V8	GND
W1	TS_PLL_REFCLKN
W12	PCIE_PVDD
W13	PCIE_AVSS
W14	GND
W15	GND
W16	GND
W17	GND
W18	GND
W19	GND
W2	TS_PLL_REFCLKP
W20	GND
W21	GND
W22	GND
W23	GND
W24	GND
W28	GND
W29	IP_PFLASH_AD8/ NAND_TYPE2
W3	TS_PLL_AVSS
W30	IP_PFLASH_AD11/NAND_PAGE1
W31	IP_PFLASH_AD13/ NOR_MEM_WIDTH1
W32	IP_PFLASH_DATA9
W33	IP_PFLASH_DATA1
W34	IP_PFLASH_DATA0
W35	IP_PFLASH_DATA8
W4	TS_PLL_VDD33
W5	PCIE_AVSS

Ball	Signal Name
W6	PCIE_RDP
W7	PCIE_RDN
W8	PCIE_AVSS
Y12	PCIE_AVSS
Y13	PCIE_AVSS
Y14	GND
Y15	GND
Y16	VDDC
Y17	VDDC
Y18	VDDC
Y19	VDDC
Y2	LED_MII_GPIO-SPI_SEL1
Y20	VDDC
Y21	VDDC
Y22	VDDC
Y23	VDDC
Y24	VDDC

Ball	Signal Name
Y28	IP_PFLASH_VDDO
Y29	IP_PFLASH_AD10/NAND_PAGE0
Y3	LED_MII_GPIO-SPI_SEL0
Y30	IP_PFLASH_AD12/ NOR_MEM_WIDTH0
Y31	IP_PFLASH_AD0
Y32	GND
Y33	IP_PFLASH_CS0_L
Y34	IP_PFLASH_REN_L
Y4	GND
Y5	PCIE_AVSS
Y6	PCIE_REFCLKN

Ball	Signal Name
Y7	PCIE_REFCLKP
Y8	PCIE_AVSS

Pin List by Signal Name

Table 17: Pin List by Singal Name - BCM56150 Devices

Signal Name	Ball
AVDD33	M12
AVS0	N4
AVSS	AC12
AVSS	AC13
AVSS	AC14
AVSS	AC15
AVSS	AC16
AVSS	AC17
AVSS	AC18
AVSS	AC19
AVSS	AC20
AVSS	AC21
AVSS	AC22
AVSS	AC23
AVSS	AC24
AVSS	AH9
AVSS	AH13
AVSS	AH14
AVSS	AH16
AVSS	AH18
AVSS	AH20
AVSS	AH22
AVSS	AH23
AVSS	AH27
AVSS	AJ4
AVSS	AJ8
AVSS	AJ12
AVSS	AJ14
AVSS	AJ16
AVSS	AJ18
AVSS	AJ20
AVSS	AJ22
AVSS	AJ24
AVSS	AJ28
AVSS	AK5

Signal Name	Ball
AVSS	AK8
AVSS	AK9
AVSS	AK10
AVSS	AK11
AVSS	AK12
AVSS	AK14
AVSS	AK15
AVSS	AK16
AVSS	AK17
AVSS	AK18
AVSS	AK19
AVSS	AK20
AVSS	AK21
AVSS	AK22
AVSS	AK24
AVSS	AK25
AVSS	AK26
AVSS	AK27
AVSS	AK28
AVSS	AK29
AVSS	AK30
AVSS	AK31
AVSS	AK32
AVSS	AL5
AVSS	AL7
AVSS	AL8
AVSS	AL10
AVSS	AL11
AVSS	AL13
AVSS	AL14
AVSS	AL16
AVSS	AL20
AVSS	AL22
AVSS	AL23
AVSS	AL25
AVSS	AL26

Signal Name	Ball
AVSS	AL28
AVSS	AL29
AVSS	AL31
AVSS	AM4
AVSS	AM6
AVSS	AM9
AVSS	AM12
AVSS	AM15
AVSS	AM18
AVSS	AM21
AVSS	AM24
AVSS	AM27
AVSS	AM30
AVSS	AM33
AVSS	AP1
AVSS	AP2
AVSS	AP34
AVSS	AP35
AVSS	AR2
AVSS	AR34
BS0_BIT_CLK	F6
BS0_PLL_AVDD33	T4
BS0_PLL_AVSS	T3
BS0_PLL_AVSS	U3
BS0_PLL_CLKN	T1
BS0_PLL_CLKP	T2
BS0_PLL_REFCLKN	U2
BS0_PLL_REFCLKP	U1
BS0_SYNC	F7
BS0_TIME_VAL	E8
BS1_BIT_CLK	E5
BS1_PLL_AVDD33	R4
BS1_PLL_AVSS	P3

Signal Name	Ball
BS1_PLL_AVSS	R3
BS1_PLL_CLKN	R1
BS1_PLL_CLKP	R2
BS1_PLL_REFCLKN	P1
BS1_PLL_REFCLKP	P2
BS1_SYNC	F8
BS1_TIME_VAL	E6
BSC_SA0	H20
BSC_SA1	H21
BSC_SCL	F20
BSC_SDA	G20
CORE_PLL_AVSS	N3
CORE_PLL_AVSS	V5
CORE_PLL_VDD33	V4
DNC	AA29
DNC	AA30
DNC	AA33
DNC	AC6
DNC	AC7
DNC	AF29
DNC	AG29
DNC	AL9
DNC	AL27
DNC	AL30
DNC	AL6
DNC	B22
DNC	C22
DNC	C32
DNC	D32
DNC	F5
DNC	N1
DNC	N2

Signal Name	Ball
DNC	N12
DNC	N13
DNC	V1
DNC	V2
EXT_QS2_CLKN	AH34
EXT_QS2_CLKP	AH35
EXT_RCVRD_CLK0	F9
EXT_RCVRD_CLK0_VLD	F10
EXT_RCVRD_CLK1	F11
EXT_RCVRD_CLK1_VLD	G9
EXT_UC_PRESENT	E7
GEN_PLL_VDD10	U12
GEN_PLL_VSS	U13
GIG_MDC	U7
GIG_MDIO	U6
GND	A2
GND	A10
GND	A13
GND	A22
GND	AA4
GND	AA14
GND	AA15
GND	AA28
GND	AA31
GND	AA32
GND	AB4
GND	AB14
GND	AB15
GND	AB16
GND	AB17
GND	AB18
GND	AB19
GND	AB20
GND	AB21
GND	AB22
GND	AB23
GND	AB24
GND	AC4
GND	AC31
GND	AC32
GND	AD6
GND	AD7
GND	AE8
GND	AF4
GND	AG8
GND	AJ5
GND	B2
GND	B7
GND	B15
GND	B17
GND	C4
GND	C12
GND	C20
GND	D1
GND	D4
GND	D6
GND	D8
GND	D9
GND	D11
GND	D14
GND	D16
GND	D18
GND	E12
GND	E15
GND	F3
GND	F4
GND	G18
GND	H8
GND	H9
GND	H10
GND	H12
GND	H14
GND	H16
GND	H18
GND	H19
GND	J2
GND	J4
GND	K8
GND	L1
GND	L4
GND	M5
GND	M8
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N5
GND	N14
GND	N15
GND	N16
GND	N17
GND	N33
GND	P4
GND	P5
GND	P8
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P29
GND	P31
GND	P32
GND	R5
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R20
GND	R21
GND	T5
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T19
GND	T20
GND	T21
GND	T22
GND	T23
GND	T24
GND	U4
GND	U5
GND	U8
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	U20
GND	U21
GND	U22
GND	U23
GND	U24
GND	U28
GND	U32
GND	V8
GND	V14
GND	V15
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18

Signal Name	Ball
GND	W19
GND	W20
GND	W21
GND	W22
GND	W23
GND	W24
GND	W28
GND	Y4
GND	Y14
GND	Y15
GND	Y32
GP_AVDDH	AH10
GP_AVDDH	AH11
GP_AVDDH	AH12
GP_AVDDH	AH24
GP_AVDDH	AH25
GP_AVDDH	AH26
GP_AVDDH	AJ9
GP_AVDDH	AJ10
GP_AVDDH	AJ11
GP_AVDDH	AJ25
GP_AVDDH	AJ26
GP_AVDDH	AJ27
GP_AVDDH	AL17
GP_AVDDH	AL18
GP_AVDDH	AL19
GP_AVDDL	AD12
GP_AVDDL	AD13
GP_AVDDL	AD14
GP_AVDDL	AD15
GP_AVDDL	AD16
GP_AVDDL	AD17
GP_AVDDL	AD18
GP_AVDDL	AD19
GP_AVDDL	AD20
GP_AVDDL	AD21
GP_AVDDL	AD22
GP_AVDDL	AD23
GP_AVDDL	AD24

Signal Name	Ball
GP0_BVDD33	AJ13
GP0_PLLVDD10	AH15
GP0_PLLVDD33	AJ15
GP0_TD0N	AH3
GP0_TD0P	AH4
GP0_TD1N	AJ2
GP0_TD1P	AJ3
GP0_TD2N	AK2
GP0_TD2P	AK1
GP0_TD3N	AK3
GP0_TD3P	AK4
GP1_BVDD33	AK13
GP1_PLLVDD10	AH17
GP1_PLLVDD33	AJ17
GP1_TD0N	AN2
GP1_TD0P	AN1
GP1_TD1N	AM2
GP1_TD1P	AM3
GP1_TD2N	AL3
GP1_TD2P	AL4
GP1_TD3N	AL1
GP1_TD3P	AL2
GP10_TD0N	AN22
GP10_TD0P	AM22
GP10_TD1N	AR23
GP10_TD1P	AP23
GP10_TD2N	AN23
GP10_TD2P	AM23
GP10_TD3N	AP24
GP10_TD3P	AN24
GP11_TD0N	AN26
GP11_TD0P	AM26
GP11_TD1N	AR26
GP11_TD1P	AP26
GP11_TD2N	AN25
GP11_TD2P	AM25
GP11_TD3N	AP25
GP11_TD3P	AR25
GP12_TD0N	AP27

Signal Name	Ball
GP12_TD0P	AN27
GP12_TD1N	AP28
GP12_TD1P	AR28
GP12_TD2N	AN28
GP12_TD2P	AM28
GP12_TD3N	AR29
GP12_TD3P	AP29
GP13_TD0N	AN31
GP13_TD0P	AM31
GP13_TD1N	AP31
GP13_TD1P	AR31
GP13_TD2N	AP30
GP13_TD2P	AN30
GP13_TD3N	AN29
GP13_TD3P	AM29
GP14_TD0N	AR32
GP14_TD0P	AP32
GP14_TD1N	AN32
GP14_TD1P	AM32
GP14_TD2N	AP33
GP14_TD2P	AN33
GP14_TD3N	AN35
GP14_TD3P	AN34
GP15_TD0N	AK34
GP15_TD0P	AK33
GP15_TD1N	AL33
GP15_TD1P	AL32
GP15_TD2N	AL35
GP15_TD2P	AL34
GP15_TD3N	AM35
GP15_TD3P	AM34
GP2_BVDD33	AJ23
GP2_PLLVDD10	AH19
GP2_PLLVDD33	AJ19
GP2_TD0N	AN3
GP2_TD0P	AN4
GP2_TD1N	AR3
GP2_TD1P	AP3
GP2_TD2N	AR4

Signal Name	Ball
GP2_TD2P	AP4
GP2_TD3N	AR5
GP2_TD3P	AP5
GP3_BVDD33	AK23
GP3_PLLVDD10	AH21
GP3_PLLVDD33	AJ21
GP3_TD0N	AN7
GP3_TD0P	AM7
GP3_TD1N	AP7
GP3_TD1P	AR7
GP3_TD2N	AP6
GP3_TD2P	AN6
GP3_TD3N	AN5
GP3_TD3P	AM5
GP4_TD0N	AR8
GP4_TD0P	AP8
GP4_TD1N	AN8
GP4_TD1P	AM8
GP4_TD2N	AP9
GP4_TD2P	AN9
GP4_TD3N	AP10
GP4_TD3P	AR10
GP5_TD0N	AP12
GP5_TD0P	AN12
GP5_TD1N	AN11
GP5_TD1P	AM11
GP5_TD2N	AR11
GP5_TD2P	AP11
GP5_TD3N	AN10
GP5_TD3P	AM10
GP6_TD0N	AP13
GP6_TD0P	AR13
GP6_TD1N	AN13
GP6_TD1P	AM13
GP6_TD2N	AR14
GP6_TD2P	AP14
GP6_TD3N	AN14
GP6_TD3P	AM14
GP7_TD0N	AR17

Signal Name	Ball
GP7_TD0P	AP17
GP7_TD1N	AN16
GP7_TD1P	AM16
GP7_TD2N	AP16
GP7_TD2P	AR16
GP7_TD3N	AP15
GP7_TD3P	AN15
GP8_TD0N	AN17
GP8_TD0P	AM17
GP8_TD1N	AP18
GP8_TD1P	AN18
GP8_TD2N	AP19
GP8_TD2P	AR19
GP8_TD3N	AN19
GP8_TD3P	AM19
GP9_TD0N	AP22
GP9_TD0P	AR22
GP9_TD1N	AP21
GP9_TD1P	AN21
GP9_TD2N	AN20
GP9_TD2P	AM20
GP9_TD3N	AR20
GP9_TD3P	AP20
GPIO0	E13
GPIO1	E14
GPIO2	F13
GPIO3	F14
GPIO4	F15
GPIO5	F16
GPIO6	F17
GPIO7	F18
IP_BOOT_DEV0	E16
IP_BOOT_DEV1	E17
IP_BOOT_DEV2	E18
IP_DDR_AD0	B16
IP_DDR_AD1	H3
IP_DDR_AD10	G3
IP_DDR_AD11	K3
IP_DDR_AD12	G2

Signal Name	Ball
IP_DDR_AD13	B19
IP_DDR_AD14	K1
IP_DDR_AD15	F2
IP_DDR_AD2	B18
IP_DDR_AD3	A16
IP_DDR_AD4	J3
IP_DDR_AD5	C17
IP_DDR_AD6	H2
IP_DDR_AD7	A17
IP_DDR_AD8	J1
IP_DDR_AD9	C19
IP_DDR_AVDD	D15
IP_DDR_BA0	C15
IP_DDR_BA1	F1
IP_DDR_BA2	A15
IP_DDR_CAS_L	C13
IP_DDR_CKE	E1
IP_DDR_CLK0_N	E3
IP_DDR_CLK0_P	D2
IP_DDR_CLK1_N	B20
IP_DDR_CLK1_P	A20
IP_DDR_CS0_L	B14
IP_DDR_CS1_L	A21
IP_DDR_DM0	A3
IP_DDR_DM1	B9
IP_DDR_DQ0	D3
IP_DDR_DQ1	C2
IP_DDR_DQ10	A4
IP_DDR_DQ11	B5
IP_DDR_DQ12	C7
IP_DDR_DQ13	B8
IP_DDR_DQ14	A7
IP_DDR_DQ15	A8
IP_DDR_DQ2	C10
IP_DDR_DQ3	C1
IP_DDR_DQ4	A11

Signal Name	Ball
IP_DDR_DQ5	B12
IP_DDR_DQ6	C9
IP_DDR_DQ7	C3
IP_DDR_DQ8	B4
IP_DDR_DQ9	C5
IP_DDR_DQS0_N	C11
IP_DDR_DQS0_P	B10
IP_DDR_DQS1_N	C6
IP_DDR_DQS1_P	B6
IP_DDR_ODT	E4
IP_DDR_RAS_L	B13
IP_DDR_RST_L	C18
IP_DDR_VDDO	A6
IP_DDR_VDDO	A14
IP_DDR_VDDO	A18
IP_DDR_VDDO	B1
IP_DDR_VDDO	B3
IP_DDR_VDDO	B11
IP_DDR_VDDO	B21
IP_DDR_VDDO	C8
IP_DDR_VDDO	C16
IP_DDR_VDDO	D5
IP_DDR_VDDO	D7
IP_DDR_VDDO	D10
IP_DDR_VDDO	D13
IP_DDR_VDDO	D17
IP_DDR_VDDO	D19
IP_DDR_VDDO	E2
IP_DDR_VDDO	G4
IP_DDR_VDDO	H1
IP_DDR_VDDO	H4
IP_DDR_VDDO	K2
IP_DDR_VDDO_CLK	D12
IP_DDR_VREF	A12
IP_DDR_WE_L	C14

Signal Name	Ball
IP_DDR_ZQ	C21
IP_MDC	E19
IP_MDIO	D20
IP_PFLASH_AD0	Y31
IP_PFLASH_AD1/WP_L	R29
IP_PFLASH_AD10/ NAND_PAGE0	Y29
IP_PFLASH_AD11/ NAND_PAGE1	W30
IP_PFLASH_AD12/ NOR_MEM_WIDTH0	Y30
IP_PFLASH_AD13/ NOR_MEM_WIDTH1	W31
IP_PFLASH_AD14/ALE	N35
IP_PFLASH_AD15/CLE	N34
IP_PFLASH_AD16	R33
IP_PFLASH_AD17	T31
IP_PFLASH_AD18	U29
IP_PFLASH_AD19	V30
IP_PFLASH_AD2/ PCIE_IF_ENABLE	R31
IP_PFLASH_AD20/ NAND_DATA_WIDTH	U31
IP_PFLASH_AD21	V31
IP_PFLASH_AD22	P33

Signal Name	Ball
IP_PFLASH_AD23	P34
IP_PFLASH_AD24/ IP_DDR_TYPE	R32
IP_PFLASH_AD3/ PCIE_RC_MODE	R30
IP_PFLASH_AD4/ PCIE_REFCLK_SEL	T29
IP_PFLASH_AD5/ PCIE_FORCE_GEN1	R28
IP_PFLASH_AD6/NAND_TYPE0	U30
IP_PFLASH_AD7/NAND_TYPE1	T30
IP_PFLASH_AD8/NAND_TYPE2	W29
IP_PFLASH_AD9/NAND_TYPE3	V29
IP_PFLASH_CS0_L	Y33
IP_PFLASH_CS1_L	M34
IP_PFLASH_DATA0	W34
IP_PFLASH_DATA1	W33
IP_PFLASH_DATA10	V34
IP_PFLASH_DATA11	V32
IP_PFLASH_DATA12	U33
IP_PFLASH_DATA13	T35
IP_PFLASH_DATA14	T32
IP_PFLASH_DATA15	R34
IP_PFLASH_DATA2	V35
IP_PFLASH_DATA3	V33
IP_PFLASH_DATA4	U34
IP_PFLASH_DATA5	T34
IP_PFLASH_DATA6	T33
IP_PFLASH_DATA7	R35
IP_PFLASH_DATA8	W35
IP_PFLASH_DATA9	W32
IP_PFLASH_RB_L	P28
IP_PFLASH_REN_L	Y34
IP_PFLASH_VDDO	T28
IP_PFLASH_VDDO	V28
IP_PFLASH_VDDO	Y28
IP_PFLASH_WEN_L	M35
JTCE	G21
JTCE1	G19
JTCK	E21
JTDI	E20
JTDO	D21
JTMS	F19
JTRST_L	F21
L1_RCVRD_CLK	E9
L1_RCVRD_CLK_BKUP	F12
L1_RCVRD_CLK_VALID	E10
L1_RCVRD_CLK_VALID_BKUP	E11
LC_PLL0_AVDD33	AD28
LC_PLL0_AVSS	AC30
LC_PLL0_AVSS	AD29
LC_PLL0_AVSS	AD32
LC_PLL0_AVSS	AJ34
LC_PLL0_AVSS	AJ35
LC_PLL0_REFCLKN	AD31
LC_PLL0_REFCLKP	AD30
LC_PLL1_AVDD33	AB28
LC_PLL1_AVSS	AB29
LC_PLL1_AVSS	AB32
LC_PLL1_AVSS	AC28
LC_PLL1_AVSS	AC29
LC_PLL1_REFCLKN	AB31
LC_PLL1_REFCLKP	AB30
LED_CLK	M7
LED_DATA/ EXT_UC_IS_SPI	M6
LED_MII_GPIO-SPI_SEL0	Y3
LED_MII_GPIO-SPI_SEL1	Y2
LED_P0_0	AE7
LED_P0_1	AE6
LED_P0_2/RXC/ GPIO8	G8
LED_P1_0	AD4
LED_P1_1	AD3
LED_P1_2/TXC/ GPIO9	G7
LED_P10_0	AG7
LED_P10_1	AF6
LED_P10_2/ TXD0/MOSI	K7
LED_P11_0	AG6
LED_P11_1	AF5
LED_P11_2/ TXD1/SS_L	K6
LED_P12_0	AH6
LED_P12_1	AG5
LED_P12_2/ TXD2	K5
LED_P13_0	AH5
LED_P13_1	AG4
LED_P13_2/ TXD3	L7
LED_P14_0	AG3
LED_P14_1	AJ6
LED_P14_2/ TXEN	L6
LED_P15_0	AK7
LED_P15_1	AK6
LED_P15_2/ TXER	L5
LED_P2_0	AD5
LED_P2_1	AE5
LED_P2_2/ RXD0/GPIO10	G6
LED_P3_0	AE1
LED_P3_1	AE2
LED_P3_2/ RXD1/GPIO11	G5
LED_P4_0	AE3
LED_P4_1	AE4
LED_P4_2/ RXD2/GPIO12	H7
LED_P5_0	AF2
LED_P5_1	AF3
LED_P5_2/ RXD3/GPIO13	H6
LED_P6_0	AG2
LED_P6_1	AG1
LED_P6_2/ RXDV/GPIO14	H5
LED_P7_0	AH2
LED_P7_1	AH1
LED_P7_2/ RXER/GPIO15	J7
LED_P8_0	AH8
LED_P8_1	AJ7

Signal Name	Ball
LED_P8_2/CRS/SCK	J6
LED_P9_0	AH7
LED_P9_1	AF7
LED_P9_2/COL/MISO	J5
LOS_0	G14
LOS_1	G15
LOS_2	G16
LOS_3	G17
OSC_XTAL_SEL	P30
PCIE_AVSS	AA5
PCIE_AVSS	AA8
PCIE_AVSS	AA13
PCIE_AVSS	AB5
PCIE_AVSS	AB8
PCIE_AVSS	AB13
PCIE_AVSS	V6
PCIE_AVSS	V7
PCIE_AVSS	V12
PCIE_AVSS	V13
PCIE_AVSS	W5
PCIE_AVSS	W8
PCIE_AVSS	W13
PCIE_AVSS	Y5
PCIE_AVSS	Y8
PCIE_AVSS	Y12
PCIE_AVSS	Y13
PCIE_CLKOUTN	AA7
PCIE_CLKOUTP	AA6
PCIE_INTR_L	G13
PCIE_PERST_L	J8
PCIE_PME_WAKE_L	G10
PCIE_PVDD	W12
PCIE_RDN	W7
PCIE_RDP	W6
PCIE_REFCLKN	Y6
PCIE_REFCLKP	Y7
PCIE_TDN	AB6
PCIE_TDP	AB7
PCIE_VDD	AA12
PCIE_VDD	AB12
QS2_AVSS	AD33
QS2_AVSS	AE28
QS2_AVSS	AE29
QS2_AVSS	AE30
QS2_AVSS	AE31
QS2_AVSS	AE32
QS2_AVSS	AE33
QS2_AVSS	AE34
QS2_AVSS	AE35
QS2_AVSS	AF33
QS2_AVSS	AG31
QS2_AVSS	AG32
QS2_AVSS	AG33
QS2_AVSS	AG34
QS2_AVSS	AG35
QS2_AVSS	AH28
QS2_AVSS	AH33
QS2_AVSS	AJ29
QS2_AVSS	AJ30
QS2_AVSS	AJ31
QS2_AVSS	AJ32
QS2_AVSS	AJ33
QS2_PVDD	AF28
QS2_PVDD	AG28
QS2_RD0N	AF34
QS2_RD0P	AF35
QS2_RD1N	AH32
QS2_RD1P	AH31
QS2_TD0N	AD34
QS2_TD0P	AD35
QS2_TD1N	AF31
QS2_TD1P	AF32
QS2_VDD	AF30
QS2_VDD	AG30
QS2_VDD	AH29
QS2_VDD	AH30
RDAC0	AL12
RDAC1	AL15
RDAC2	AL21
RDAC3	AL24
SFLASH_CLK	P7
SFLASH_CS_L	N6
SFLASH_IO0	P6
SFLASH_IO1	N7
SFLASH_IO2	R6
SFLASH_IO3	R7
SYS_RST_L	K4
TS_GPIO0	G11
TS_GPIO1	G12
TS_PLL_AVSS	V3
TS_PLL_AVSS	W3
TS_PLL_REFCLKN	W1
TS_PLL_REFCLKP	W2
TS_PLL_VDD33	W4
UART1_CTS_L	AB2
UART1_DCD_L	AA3
UART1_DSR_L	AB3
UART1_DTR_L	AA2
UART1_RI_L	AA1
UART1_RTS_L/SFLASH_BYTE_ADDR	AB1
UART1_RX	AC3
UART1_TX	AC2
UART2_RX	AD1
UART2_TX	AD2
VDD_SENSE	T18
VDD33	AD8
VDD33	AF8
VDD33	H11
VDD33	H13
VDD33	H15
VDD33	H17
VDD33	L8
VDD33	N8
VDD33	R8
VDDC	AA16
VDDC	AA17
VDDC	AA18
VDDC	AA19
VDDC	AA20
VDDC	AA21
VDDC	AA22
VDDC	AA23
VDDC	AA24
VDDC	V16
VDDC	V17
VDDC	V18
VDDC	V19
VDDC	V20
VDDC	V21
VDDC	V22
VDDC	V23
VDDC	V24
VDDC	Y16
VDDC	Y17
VDDC	Y18
VDDC	Y19
VDDC	Y20
VDDC	Y21
VDDC	Y22
VDDC	Y23
VDDC	Y24
VSS_SENSE	T17
WC_AVSS	A23
WC_AVSS	A25
WC_AVSS	A27
WC_AVSS	A29
WC_AVSS	A31
WC_AVSS	A34
WC_AVSS	B23
WC_AVSS	B25
WC_AVSS	B27

Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball
WC_AVSS	B29	WC_AVSS	F28	WC_AVSS	L31	WC0_RD3P	M30
WC_AVSS	B31	WC_AVSS	F30	WC_AVSS	L32	WC0_REFCLKN	A33
WC_AVSS	B32	WC_AVSS	F32	WC_AVSS	L33	WC0_REFCLKP	A32
WC_AVSS	B33	WC_AVSS	F33	WC_AVSS	L34	WC0_RVDD10	M23
WC_AVSS	B34	WC_AVSS	F34	WC_AVSS	L35	WC0_RVDD10	M24
WC_AVSS	B35	WC_AVSS	F35	WC_AVSS	M18	WC0_TD0N	J35
WC_AVSS	C23	WC_AVSS	G23	WC_AVSS	M20	WC0_TD0P	J34
WC_AVSS	C24	WC_AVSS	G24	WC_AVSS	M22	WC0_TD1N	G34
WC_AVSS	C25	WC_AVSS	G25	WC_AVSS	M28	WC0_TD1P	G35
WC_AVSS	C26	WC_AVSS	G26	WC_AVSS	M29	WC0_TD2N	E34
WC_AVSS	C27	WC_AVSS	G27	WC_AVSS	M32	WC0_TD2P	E35
WC_AVSS	C28	WC_AVSS	G28	WC_AVSS	M33	WC0_TD3N	C34
WC_AVSS	C29	WC_AVSS	G29	WC_AVSS	N18	WC0_TD3P	C35
WC_AVSS	C30	WC_AVSS	G30	WC_AVSS	N20	WC0_TVDD10	P23
WC_AVSS	C31	WC_AVSS	G31	WC_AVSS	N22	WC0_TVDD10	P24
WC_AVSS	C33	WC_AVSS	G32	WC_AVSS	N23	WC1_PVDD10	H25
WC_AVSS	D22	WC_AVSS	G33	WC_AVSS	N24	WC1_PVDD10	H26
WC_AVSS	D23	WC_AVSS	H23	WC_AVSS	N28	WC1_RD0N	E29
WC_AVSS	D24	WC_AVSS	H24	WC_AVSS	N29	WC1_RD0P	F29
WC_AVSS	D25	WC_AVSS	H27	WC_AVSS	N30	WC1_RD1N	E27
WC_AVSS	D26	WC_AVSS	H28	WC_AVSS	N31	WC1_RD1P	F27
WC_AVSS	D27	WC_AVSS	H29	WC_AVSS	N32	WC1_RD2N	E25
WC_AVSS	D28	WC_AVSS	H32	WC_AVSS	P18	WC1_RD2P	F25
WC_AVSS	D29	WC_AVSS	H33	WC_AVSS	P19	WC1_RD3N	E23
WC_AVSS	D30	WC_AVSS	H34	WC_AVSS	P20	WC1_RD3P	F23
WC_AVSS	D31	WC_AVSS	H35	WC_AVSS	P21	WC1_REFCLKN	G22
WC_AVSS	D33	WC_AVSS	J28	WC_AVSS	P22	WC1_REFCLKP	H22
WC_AVSS	D34	WC_AVSS	J29	WC_AVSS	R22	WC1_RVDD10	M21
WC_AVSS	D35	WC_AVSS	J30	WC_AVSS	R23	WC1_RVDD10	N21
WC_AVSS	E22	WC_AVSS	J31	WC_AVSS	R24	WC1_TD0N	B24
WC_AVSS	E24	WC_AVSS	J32	WC0_PVDD10	K28	WC1_TD0P	A24
WC_AVSS	E26	WC_AVSS	J33	WC0_PVDD10	L28	WC1_TD1N	A26
WC_AVSS	E28	WC_AVSS	K29	WC0_RD0N	E31	WC1_TD1P	B26
WC_AVSS	E30	WC_AVSS	K32	WC0_RD0P	F31	WC1_TD2N	B28
WC_AVSS	E32	WC_AVSS	K33	WC0_RD1N	H31	WC1_TD2P	A28
WC_AVSS	E33	WC_AVSS	K34	WC0_RD1P	H30	WC1_TD3N	B30
WC_AVSS	F22	WC_AVSS	K35	WC0_RD2N	K31	WC1_TD3P	A30
WC_AVSS	F24	WC_AVSS	L29	WC0_RD2P	K30	WC1_TVDD10	M19
WC_AVSS	F26	WC_AVSS	L30	WC0_RD3N	M31	WC1_TVDD10	N19

Signal Name	Ball
XG_MDC	T7
XG_MDIO	T6
XG_PLL2_AVDD33	M3
XG_PLL2_AVSS	AC5
XG_PLL2_AVSS	AC8
XG_PLL2_AVSS	L2
XG_PLL2_AVSS	L3
XG_PLL2_AVSS	M4

Signal Name	Ball
XG_PLL2_REFCLKN	M1
XG_PLL2_REFCLKP	M2
XG_VDDO	T8
XTAL_AVDD	AB33
XTAL_AVSS	AA34
XTAL_AVSS	AA35
XTAL_AVSS	AC33
XTAL_AVSS	AC34

Signal Name	Ball
XTAL_AVSS	AC35
XTALN	AB34
XTALP	AB35

Section 8: Electrical Specifications

Absolute Maximum Ratings

The specifications shown in Table 19 indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 18: Absolute Maximum Ratings

Parameter	*Symbol*	*Min.*	*Max.*	*Units*	*Notes*
1.00V, Core Voltage	–	–0.50	+1.37	V	–
1.00V, Analog Voltage	–	–0.40	+1.37	V	–
1.20V, I/O Voltage	–	–0.50	+1.50	V	–
1.525V, I/O Voltage	–	–0.50	+1.80	V	–
1.80V, I/O Voltage	–	–0.50	+2.10	V	–
3.30V, I/O Voltage	–	–0.50	+4.10	V	–
Storage Temperature	T_{STG}	–40	+125	°C	–
Electrostatic Discharge (ESD) (non-SerDes pins)	V_{ESD}	–	–	–	–
– Human Body Model (HBM) per EIA/JESD22-A114-E		–	±2000	V	–
– Machine Model (MM) per EIA/JESD-A115-A		–	±100	V	–
– Charge Device Model (CDM) per EIA/JESD22-C101C		–	±300	V	–
ESD (PCIe, Warpcore Technology, and QSGMII SerDes pins)	V_{ESD}	–	–	–	–
– Human Body Model per EIA/JESD22-A114-E		–	±1400	V	–
– Machine Model per EIA/JESD-A115-A		–	±75	V	–
– Charge Device Model per EIA/JESD22-C101C		–	±200	V	–

DC Characteristics

Operating Conditions

Broadcom recommends operating the BCM56150 under the following conditions shown in Table 19.

Table 19: Operating Conditions

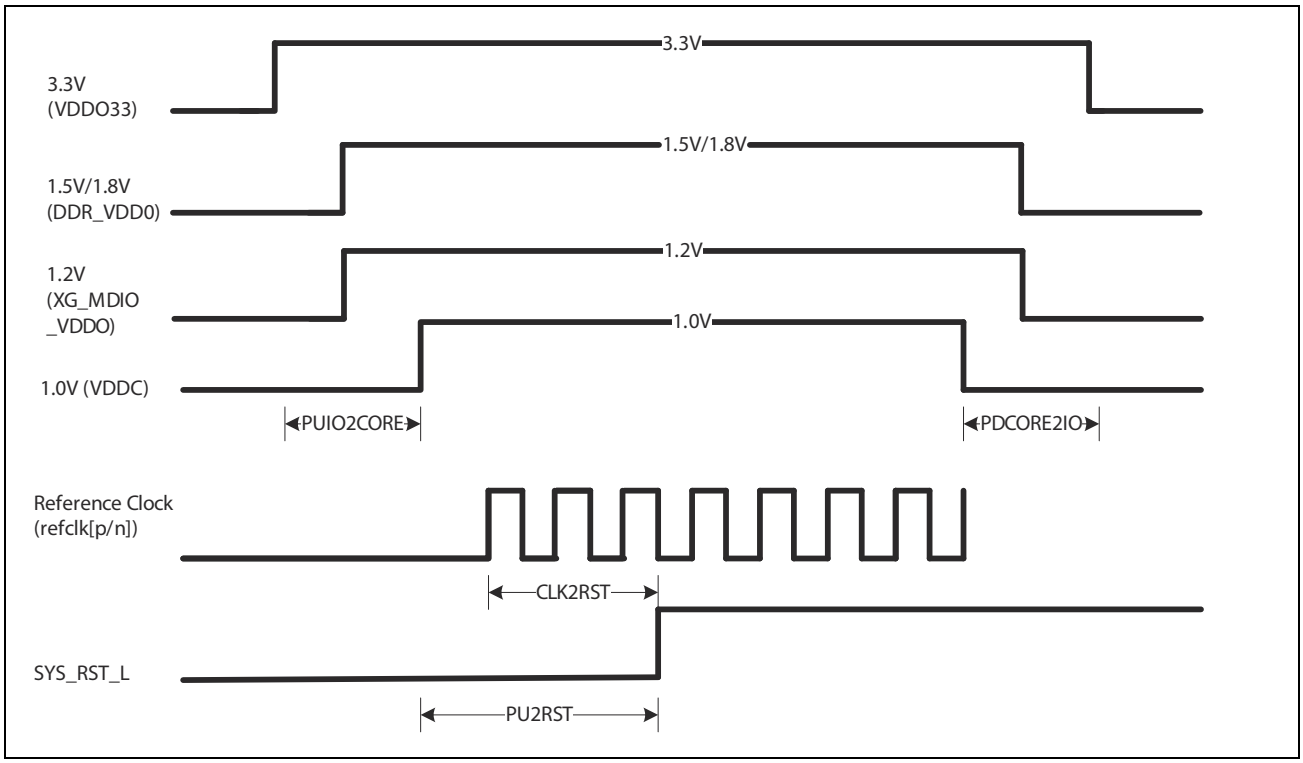
Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
1.00V ±2%, Core Voltage	–	0.980	1.00	1.020	V
1.00V ±2%, Analog Voltage	–	0.980	1.00	1.020	V
1.20V ±3%, I/O Voltage	–	1.164	1.20	1.236	V
1.50V ±5%, I/O Voltage	–	1.425	1.50	1.575	V
1.80V ±5%, I/O Voltage	–	1.710	1.800	1.890	V
3.30V ±5%, I/O Voltage	–	3.135	3.30	3.465	V
Ambient Temperature	T_A	0	–	70	°C
Ambient Temperature (Industrial Temperature)	T_A	–40	–	+85	°C
Junction Temperature[a]	T_J	–	–	125	°C

a. Device must not operate at Maximum junction temperature 125°C for extended periods of time. Steady state temperature is 110°C.

Power-Up and Power-Down Specifications

The power-up and power-down requirements for the BCM56150 are outlined in Figure 22. Violating sequencing can cause latch-up damage to the device.

Figure 22: Power-Up and Power-Down Timing



Note: When a crystal is used as the external clock source, there is no CLK2RST requirement.

Table 20: AC Specifications for Power-Up and Power-Down

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
$t_{PUIO2CORE}$	*VDDO (3.3, 1.5/1.8, 1.2) to VDDC/Analog PWR (1.0V) power-up time*	0	–	5	ms	1
$t_{PDCORE2IO}$	*VDDO (3.3, 1.5/1.8, 1.2) to VDDC/Analog PWR (1.0V) power-down time*	0	–	–	ms	1, 4
t_{PU2RST}	*All voltages at valid operating conditions to the deassertion of sys_rst_n*	40	–	–	ms	1, 3
$t_{CLK2RST}$	*All clocks valid to the deassertion of sys_rst_n*	t_{PU2RST} – 5	–	–	ms	2, 3
$t_{COR2LCK}$	*Time for the core clock to internally become valid and allow register accesses*	1	–	–	ms	2, 3
t_{RAMP}	Ramp time for each voltage rail 10% to 90%	0	–	5	ms	–

Table 20: AC Specifications for Power-Up and Power-Down

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes

Note:

1. Valid operating conditions are listed in Table 19 on page 114.
2. Valid clocks are described in the AC Characteristics section.
3. Ensures lock time on internal PLL.
4. The power-down has no sequencing requirements and no time limit to parameter $t_{PDCORE2IO}$.
5. The VDDC (1.0V core) must be powered up at the same time or before the GP_AVDDL (1.0V analog) supply.

Power Supply Current

Table 21: BCM56150 Power Supply Current for 24P 1G + 4P 10G at 110°C Junction Temperature

Parameter	Voltage (V)	Current (A)	Power (W)
1.0V Digital	1.02	6.98	7.12
1.0V Analog	1.02	1.48	1.50
1.2V/2.5V/3.3V MDIO	2.55	0.02	0.05
1.5V DDR3-667	1.53	0.32	0.49
3.3V	3.37	1.08	3.65
Total			12.81

Table 22: BCM56150 Power Supply Current for 24P 1G + 2P 10G + 2P 13G at 110°C Junction Temperature

Parameter	Voltage (V)	Current (A)	Power (W)
1.0V Digital	1.02	7.65	7.80
1.0V Analog	1.02	1.79	1.82
1.2V/2.5V/3.3V MDIO	2.55	0.02	0.05
1.5V DDR3-667	1.53	0.32	0.49
3.3V	3.37	1.09	3.67
Total			13.83

Standard 3.3V Signals

The specifications shown in Table 23 apply to all CMOS 3.3V general I/O signals, along with Synchronous Ethernet Interface, BroadSync, NAND Flash, UART, GPIO, JTAG, and LED signals, except for BSC and MDIO/MDC.

Table 23: Standard 3.3V Signals

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Input Voltage	V_{IN}	–0.25	–	+3.63	V
Input Low Voltage	V_{IL}	–	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	–	V
Input Leakage Current	I_I	–15	–	+15	µA
Output Low Voltage	V_{OL}	–	–	0.4	V
Output High Voltage	V_{OH}	VDDO33–0.4	–	–	V
I/O Pin Capacitance (GBD)	C_I	–	–	TBD	pF

PCIe DC Characteristics

Table 24: PCIe DC Characteristics

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Transmitter					
Output Impedance (Differential)	R_{OUT}	–	100	–	Ω
Output Voltage (Differential pk-pk)	V_{OD}	800	–	1200	mVp-p
Receiver					
Input Impedance (Differential)	RIN	–	100	–	Ω
Input Voltage (Differential pk-pk)	VID	175	–	2000	mVp-p

BSC Signals

BSC_SCL and BSC_SDA are bidirectional open-drain signals. An external pull-up to 3.3V should be provided on the board. BSC_SA1 and BSC_SA0 are standard 3.3V signals. It is recommended that they be pulled high to 3.3V or left unconnected.

Table 25: BSC Signals[a]

Parameter	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Units*
Input Voltage	V_{IN}	–	–0.25	–	+3.63	V
Input Low Voltage	V_{IL}	–	–	–	0.3*VDDO[b]	V
Input High Voltage	V_{IH}	–	0.7*VDDO[b]	–	–	V
Input Leakage Current	I_I	–	–10	–	+10	µA
Output Low Voltage	V_{OL}	I_{OL} = 3 mA	–	–	0.4	V
Hysteresis of Schmitt Inputs (GBD)	V_{HYS}	–	0.18	–	–	V
I/O Pin Capacitance (GBD)	C_I	–	–	–	TBD	pF

a. BSC I/Os are true open-drain type and require external pull-up resistors.
b. VDDO is 3.3V external pull-up supply.

SGMII/SerDes Signals

Table 26: SGMII/SerDes DC Characteristics

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Receiver					
Input Voltage (Differential pk-pk), AC-coupled	V_{ID}	100	–	–	mVp-p
Input Impedance (Differential), integrated on-chip	R_{IN}	80	100	120	Ω
Transmitter					
Output Voltage (Differential pk-pk), programmable	V_{OD}	0	–	1100	mVp-p
Output Impedance (Differential)	R_{OUT}	80	100	120	Ω
Preemphasis (1-Vmin/Vmax)	–	0	–	66	%

2.5GbE SerDes Signals

Table 27: 2.5GbE SerDes DC Characteristics

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Differential Input Voltage (Warpcore)	VIN	100	–	1600	mVppd
Differential Input Impedance	VRIN	–	100	–	Ω
Differential Output Voltage	VOD	600	–	1200	mVppd
Differential Output Impedance	VROUT	–	100	–	Ω

QSGMII SerDes Signals

Table 28: QSGMII SerDes DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Receiver					
RX Baud Rate	R_Baud	–	5.0	–	GSym/s
Input Differential Voltage	R_Vdiff	100	–	900	mVppd
Differential Resistance	R_Rdin	85	100	115	Ω
Bias Voltage Source Impedance (Load Type 2)	R_Zvtt	–	–	30	Ω
Transmitter					
Output Differential Voltage (into floating Load Rload=100Ω)	T_Vdiff	400	550	900	mVppd
Differential Resistance	T_Rd	85	100	115	Ω
Recommended Output Rise and Fall Times (20% to 80%)	5 Gps 3 Gps 1.25 Gps	30 67 100	78 136 200	–	ps

Warpcore Technology Quad SerDes Signals

Table 29: Warpcore Technology Quad SerDes DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Receiver					
Input Voltage (Differential pk-pk), AC-coupled	V_{ID}	100	–	1600	mVp-p
Input Impedance (Differential), integrated on-chip	R_{IN}	80	100	120	Ω
Transmitter					
Output Voltage (Differential pk-pk), programmable	V_{OD}	700	100	1100	mVp-p
Output Impedance (Differential)	R_{OUT}	–	100	–	Ω

Table 30: Warpcore Technology SerDes Specifications

Mode	Specification	Functionality
XFI	XFP MSA	Per the specification except for Return Loss. Fully compliant with XFI+ standard.
SFI (10GBASE-SR/ LR)	SFF-8431	–
SGMII	Cisco's ENG-46158	Per the specification
1000BASE-X	IEEE 802.3z	Per the specification
10GBASE-KR	IEEE 802.3AP	10G backplane

MIIM (MDIO) Signals

Table 31: MIIM (XG) (Clause 45 Electrical Characteristics)

Parameter	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Units*
Input Voltage	V_{IN}	–	-0.25	–	+1.5	V
Input Low Voltage	V_{IL}	–	–	–	0.36	V
Input High Voltage	V_{IH}	–	0.84	–	–	V
Input Leakage Current	I_I	–	–10	–	+10	µA
Output Low Voltage	V_{OL}	I_{OL} = 100 µA	–	–	0.2	V
Output Low Current	I_{OL}	V_{OL} = 0.2V	4.0	–	–	mA
Output High Voltage	V_{OH}	I_{OH} = -100 µA	1.0	–	–	V
I/O Pin Capacitance (GBD)	C_I	–	–	–	TBD	pF
Note: GBD = Guaranteed by design are parameters that are not tested.						

Table 32: MIIM (Clause 22 Electrical Characteristics)

Parameter	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Units*
Input Voltage	V_{IN}	–	–0.3	–	+3.6	V
Input Low Voltage	V_{IL}	–	–	–	0.8	V
Input High Voltage	V_{IH}	–	2.0	–	–	V
Input Leakage Current	I_I	–	–15	–	+15	µA
Output Low Voltage	V_{OL}	I_{OL} = 11 mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –11 mA	V_{DDO} - 0.4	–	–	V
I/O Pin Capacitance (GBD)	C_I	–	–	–	TBD	pF
Note: GBD = Guaranteed by design are parameters that are not tested.						

AC Characteristics

MII Interface Timing

This section shows timing information for the MII Interface pins.

MII Input Timing

Figure 23: MII Input Timing

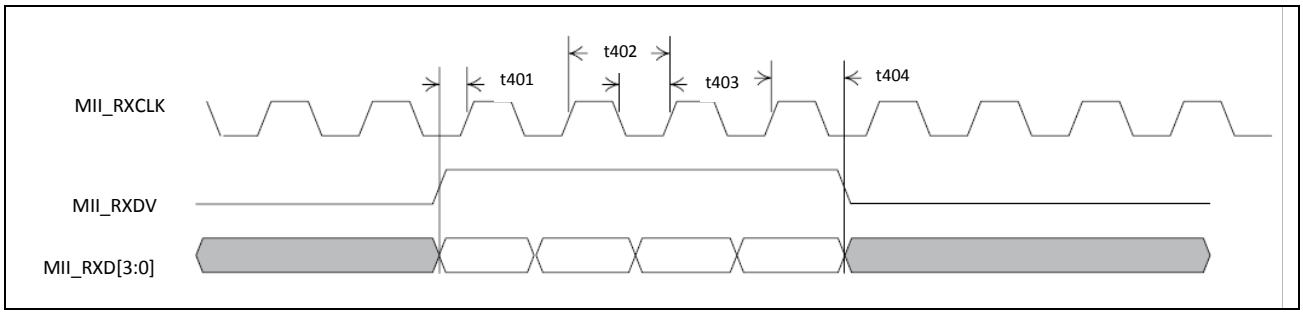


Table 33: MII Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
t401	MII_RXDV, MII_RXD[3:0] to MII_RXCLK rising setup time	5	–	–	ns
t402	MII_RXC clock period (100BASE-TX mode)	–	40	–	ns
t403	MII_RXCLK high/low time (100BASE-TX mode)	16	–	24	ns
t404	MII_RXDV, MII_RXD[3:0] to MII_RXCLK rising hold time	10	–	–	ns
–	Duty cycle	40	50	60	%

MII Output Timing

Figure 24: MII Output Timing

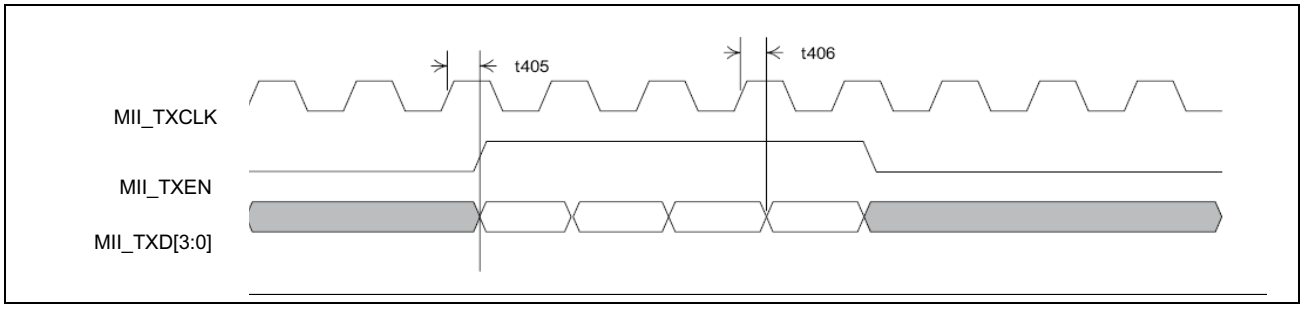


Table 34: MII Output Timing

Parameter	Description	Min	Typ	Max	Units
t405	MII_TXCLK high to MII_TXEN, MII_TXD[3:0] valid	4	–	15	ns
t406	MII_TXCLK high to MII_TXEN, MII_TXD[3:0] invalid (hold)	4	–	–	ns

AC Timing for Reset

The *SYS_RST_L* signal is synchronized internal to the IC and, as such, asynchronous assertion and deassertion are acceptable.

BSC AC Characteristics

The BSC interface can be operated in two modes:

- Slave mode
- CPU-controlled master/slave mode

The external master drives BSC_SDA during a write operation and samples BSC_SDA during a read operation.

Figure 25: BSC Timing Diagram

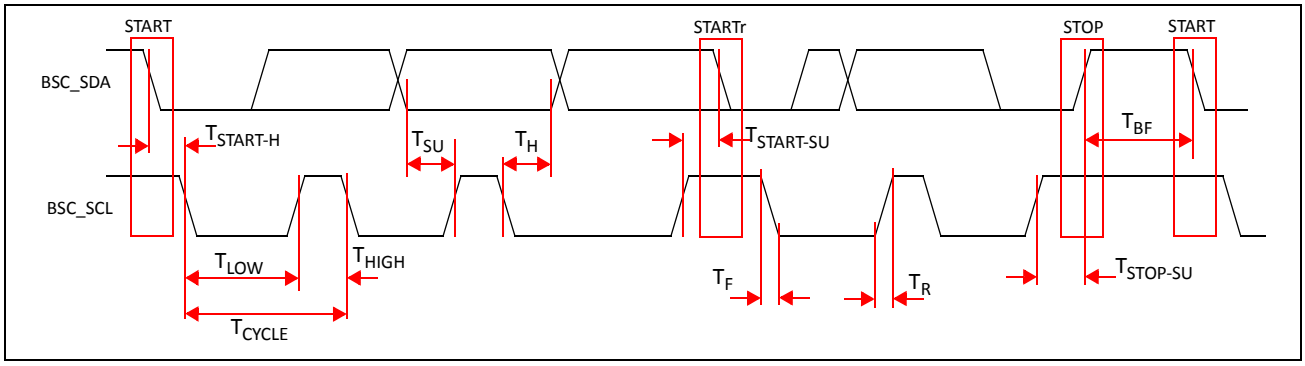


Table 35: BSC Master/Slave Fast-Mode Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
BSC_SCL Cycle Time	T_{CYCLE}	2.5	–	–	µs
BSC_SCL Low Time	T_{LOW}	1.3	–	–	µs
BSC_SCL High Time	T_{HIGH}	0.6	–	–	µs
Data Hold Time	T_{H}	0	–	–	µs
Data Setup Time	T_{SU}	100	–	–	ns
Rise Time, Clock and Data (See Note)	T_{R}	–	–	300	ns
Fall Time, Clock and Data (GBD)	T_{F}	–	–	300	ns
Hold Time, START or repeated START	$T_{START–H}$	0.6	–	–	µs
Setup Time, repeated START	$T_{START–SU}$	0.6	–	–	µs
Setup Time, STOP	$T_{STOP–SU}$	0.6	–	–	µs
Bus Free Time (Between STOP and START)	T_{BF}	1.3	–	–	µs

Table 36: BSC Master/Slave Standard-Mode Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
BSC_SCL Cycle Time	T_{CYCLE}	2.5	–	–	µs
BSC_SCL Low Time	T_{LOW}	1.3	–	–	µs
BSC_SCL High Time	T_{HIGH}	0.6	–	–	µs
Data Hold Time	T_{H}	0	–	–	µs
Data Setup Time	T_{SU}	100	–	–	ns
Rise Time, Clock and Data (See Note)	T_{R}	–	–	300	ns
Fall Time, Clock and Data (GBD)	T_{F}	–	–	300	ns
Hold Time, START or repeated START	$T_{START–H}$	0.6	–	–	µs
Setup Time, repeated START	$T_{START–SU}$	0.6	–	–	µs
Setup Time, STOP	$T_{STOP–SU}$	0.6	–	–	µs
Bus Free Time (Between STOP and START)	T_{BF}	1.3	–	–	µs

Note: BSC_SCL and BSC_SDA are open-drain outputs. The rise time is dependent on the strength of the external pull-up resistor, which should be chosen to meet the rise time requirement.

The BCM56150 device drives the BSC_SCL clock, with a programmable speed of 100 kHz or 400 kHz based on the mode bit called MODE_400. The BCM56150 drives BSC_SDA during a write operation and samples BSC_SDA during a read operation.

SPI AC Characteristics

The SPI interface can be operated in two modes:

- Master mode
- Slave mode

Figure 26: SPI Interface Master Mode Timing Diagram

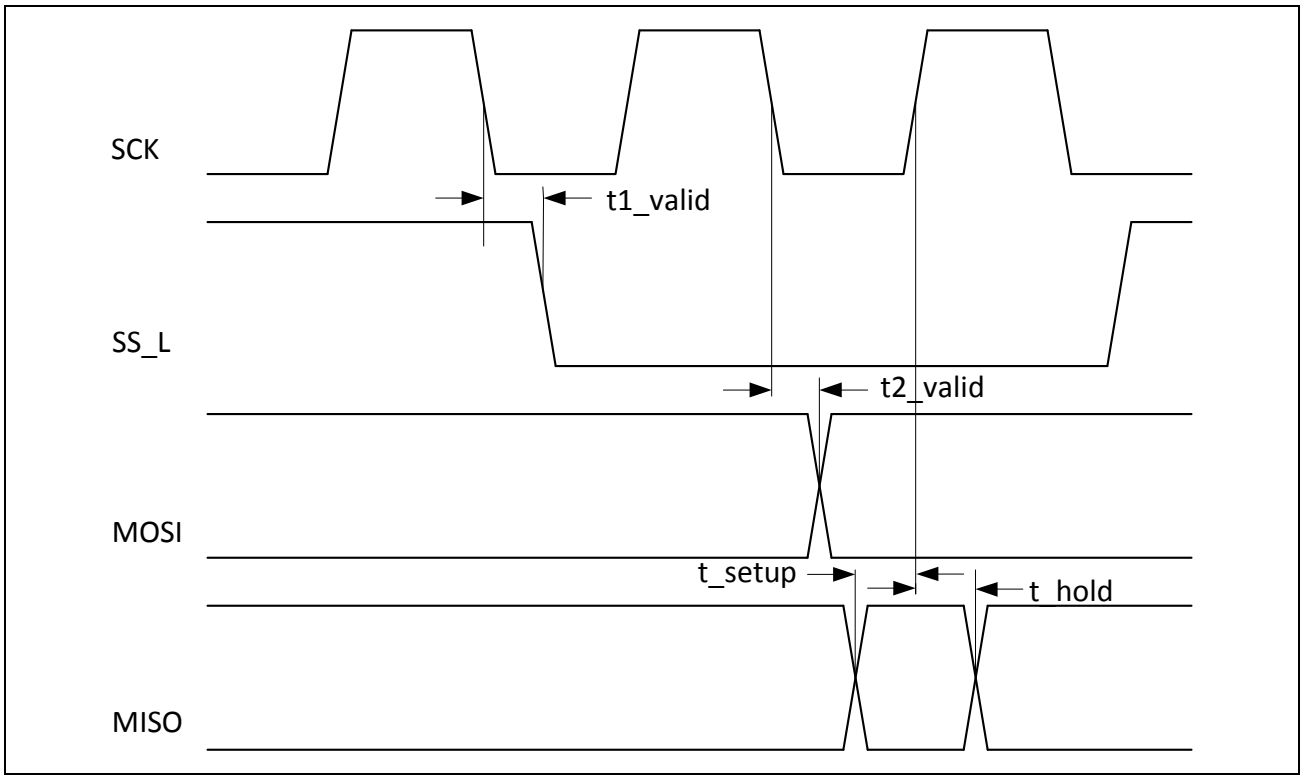


Table 37: SPI Master Mode Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
SCK Cycle Time	T_{CYCLE}	32	–	–	ns
SS_L Valid Time	t1_valid	5	–	–	ns
MOSI Valid Time	t2_valid	5	–	–	ns
MISO Setup Time	t_setup	5	–	–	ns
MISO Hold Time	t_hold	0	–	–	ns

Figure 27: SPI Interface Slave Mode Timing Diagram

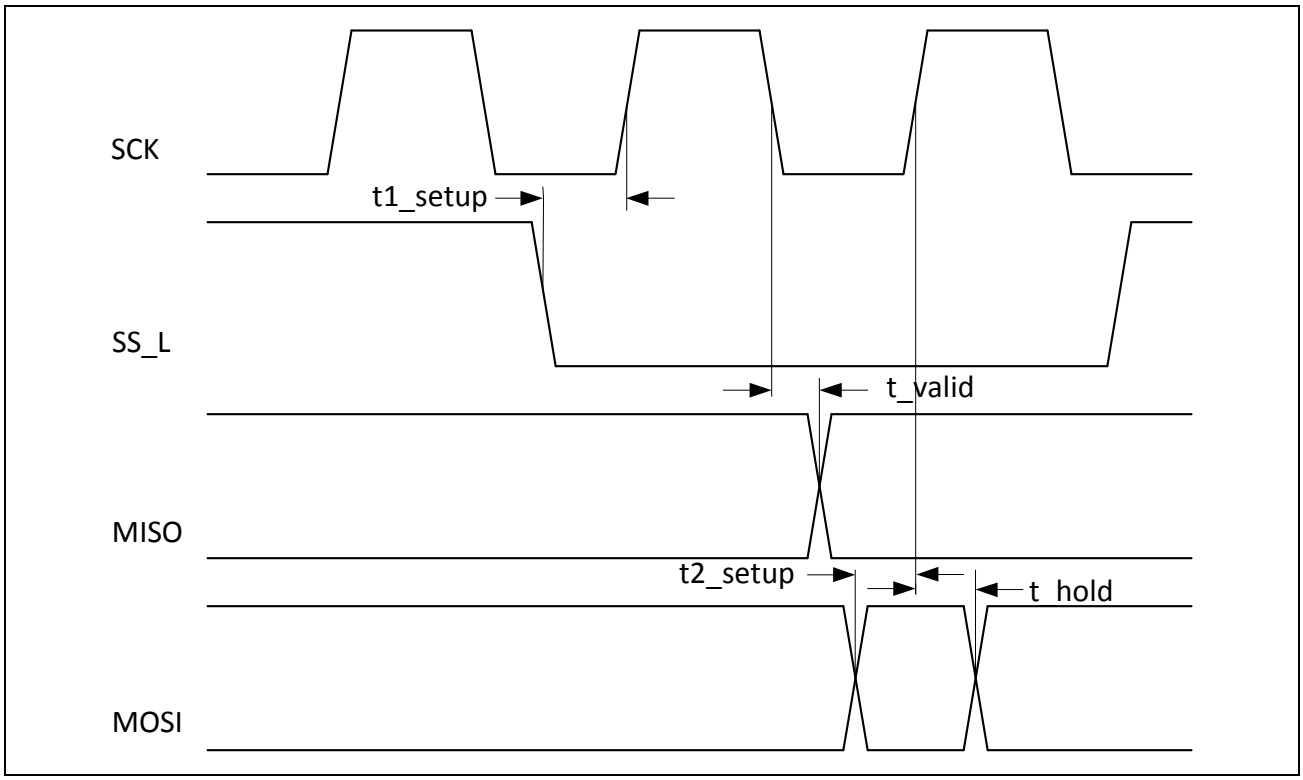


Table 38: SPI Slave Fast Mode Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
SCK Cycle Time	T_{CYCLE}	32	–	–	ns
SS_L Setup Time	t1_setup	4	–	–	ns
MOSI Setup Time	t2_setup	4	–	–	ns
MOSI Hold Time	t_hold	4	–	–	ns
MISO Valid Time	t_valid	9	–	–	ns

MDIO AC Characteristics

Figure 28: MIIM Interface Timing Diagram

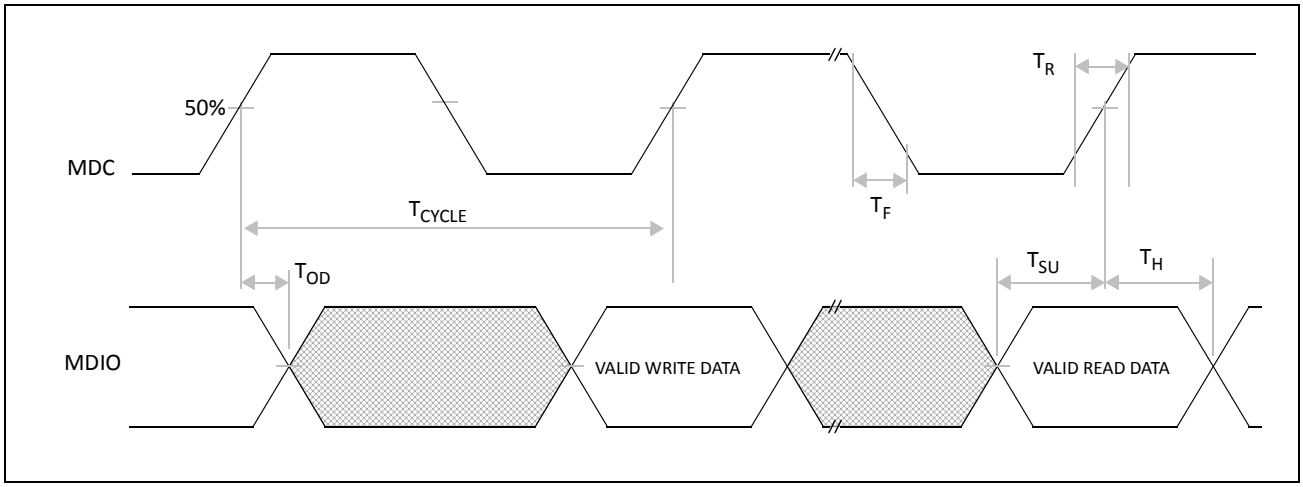


Table 39: MDC/MDIO Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
MDC Cycle Time	T_{CYCLE}	80	400	–	ns
MDC Duty Cycle	–	40	–	60	%
MDC Rise/Fall Time (Requirement 20%–80%)	T_R, T_F	–	–	10	ns
MDIO Setup Time	T_S	20	–	–	ns
MDIO Hold Time	T_H	10	–	–	ns
MDIO Output Delay	T_{OD}	0	–	25	ns

JTAG AC Specifications

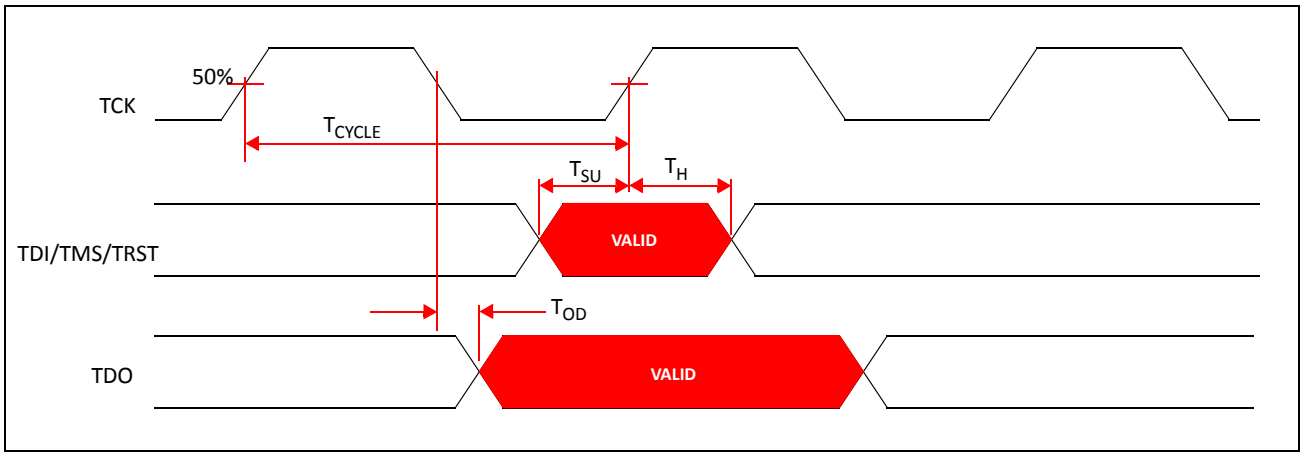
Table 40: AC Characteristics for JTAG

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
j_tck cycle time	t_{CYCLE}	80.0	–	–	ns
j_tck falling edge to output valid. Applicable to *j_tdo.*	t_{OD}	0	–	25	ns
Data input setup time before *j_tck*. Applicable to *j_tdi and j_tms.*	t_{SU_JT}	15	–	–	ns
Data hold time after *j_tck* rise Applicable to *j_tdi and j_tms.*	t_{H_JT}	5	–	–	ns
Input setup time before *j_tck* rising edge. Applicable to *j_trst.*	t_{SU_JTRS}	15	–	–	ns
Input hold time after *j_tck* rising edge. Applicable to *j_trst.*	t_{H_JTRS}	5	–	–	ns

Note: Unless otherwise noted, the specifications are valid across the following operating conditions:

- The threshold value is at 50% of the applicable I/O rail voltage.
- The default loading on an output is 5 pF.

Figure 29: JTAG Timing



NAND Flash Interface Timing

The BCM56150 is Open NAND Flash Interface (ONFI)-compliant with the NAND Flash interface, supporting single-level cell (SLC)/multi-level cell (MLC) devices with on-chip error-correction code (ECC).

This section contains timing for the following operations:

- Command latch cycle timing
- Address latch cycle timing
- Read cycle timing
- Write cycle timing

Figure 30: NAND Flash Command Latch Cycle Timing

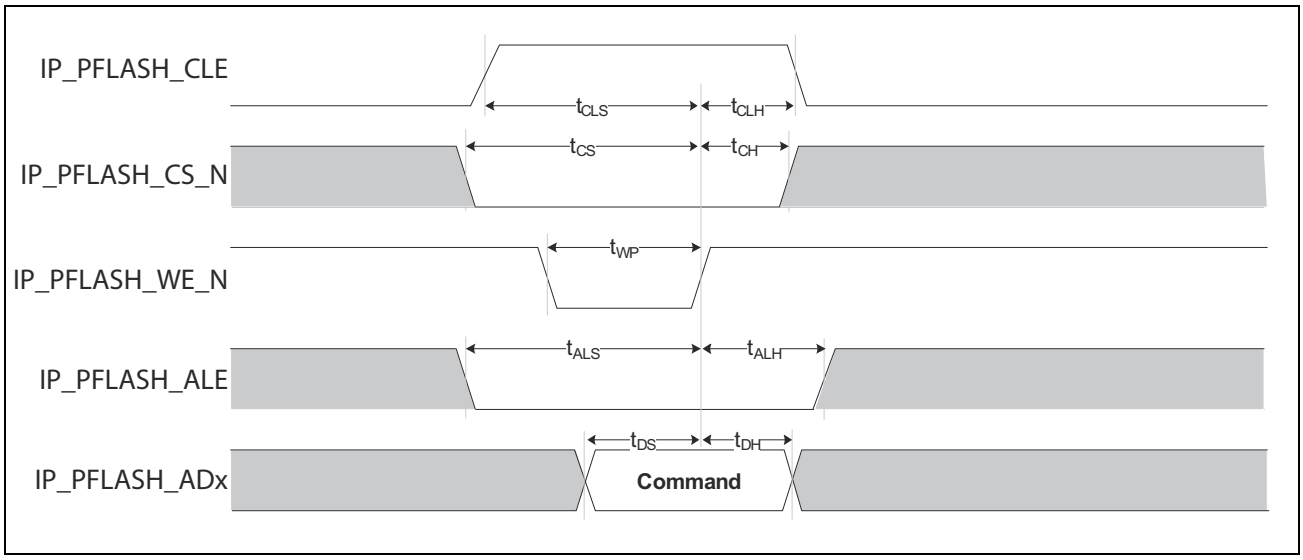


Figure 31: NAND Flash Address Latch Cycle Timing

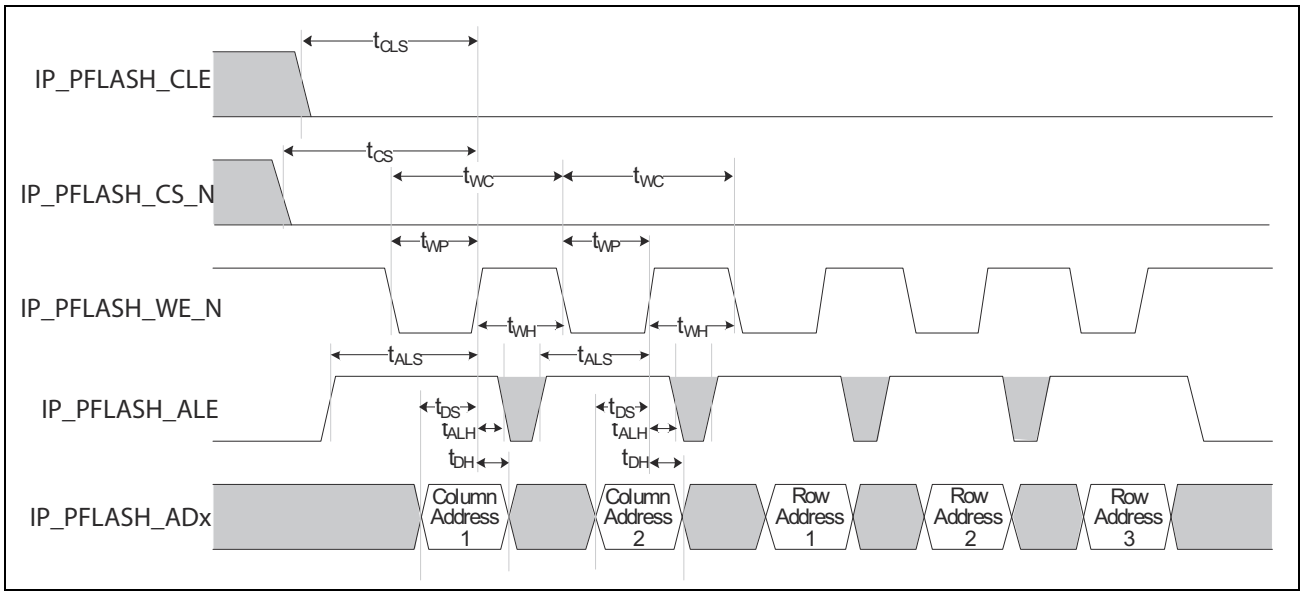
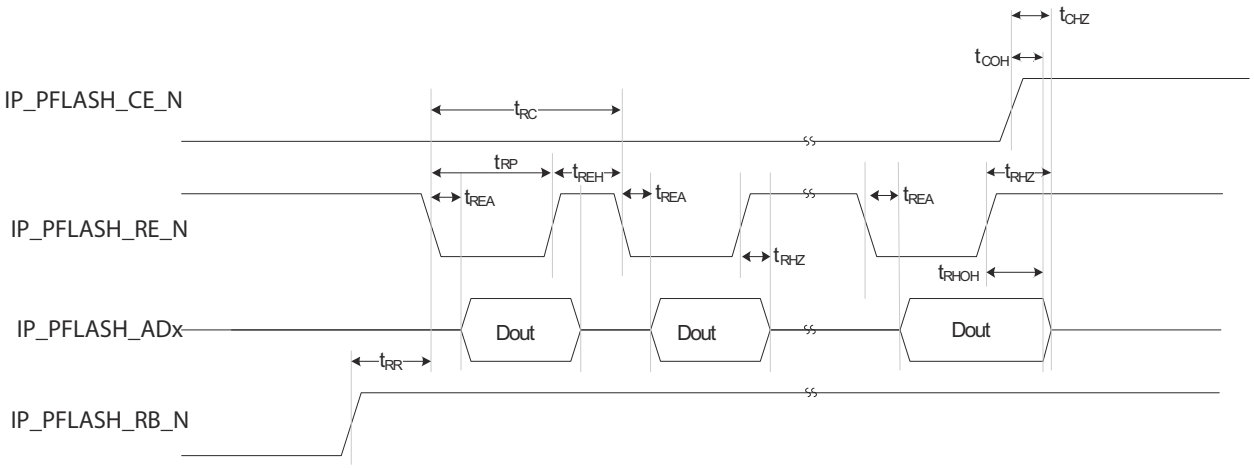


Figure 32: NAND Flash Read Cycle Timing



Notes:

1. Transition is measured at +/-200 mV from steady state voltage with load.
2. These parameters are sampled and not 100% tested.
3. t_{RHOH} starts to be valid when the frequency is lower than 20 MHz.
4. NAND_CLE, NAND_WE_L, and NAND_ALE = L.

Figure 33: NAND Flash Write Cycle Timing

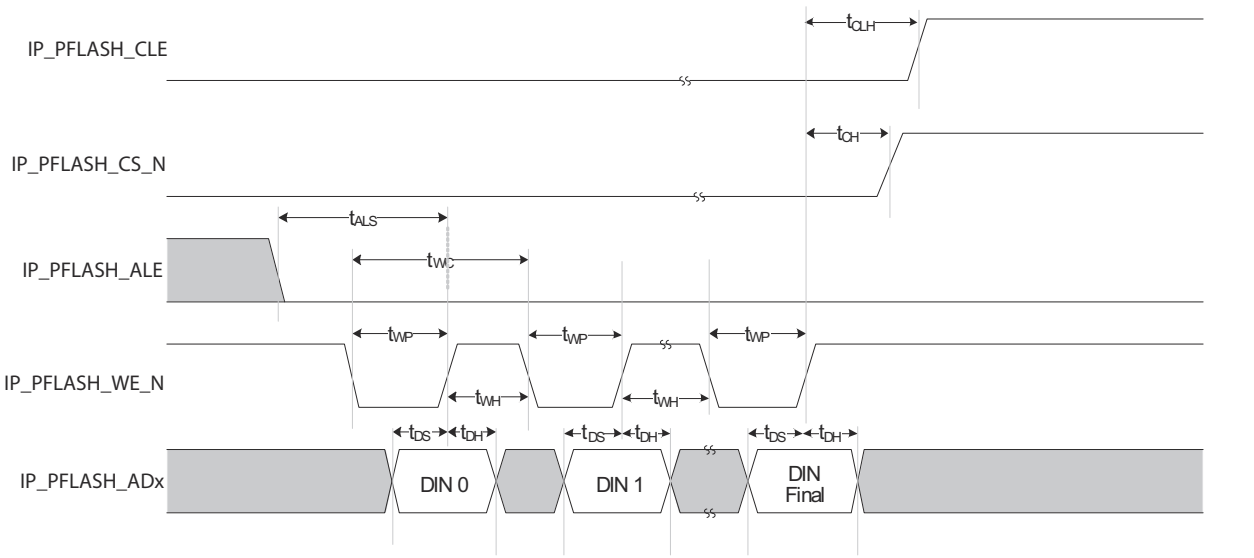


Table 41: NAND Flash Timing Characteristics for Command, Address, and Data Input[a]

Parameter	Symbol	ONFI Mode0 Min.	ONFI Mode1 Min.	ONFI Mode2 Min.	ONFI Mode3 Min.	ONFI Mode4 Min.	ONFI Mode5 Min.	Unit
IP_PFLASH_CLE setup time	t_{CLS}[b]	50	–	–	–	–	–	ns
IP_PFLASH_CLE hold time	t_{CLH}	20	–	–	–	–	–	ns
IP_PFLASH_CS_N setup time	t_{CS}[b]	70	–	–	–	–	–	ns
IP_PFLASH_CS_N hold time	t_{CH}	5	–	–	–	–	–	ns
IP_PFLASH_WE_N pulse width	t_{WP}	50	–	–	–	–	–	ns
IP_PFLASH_ALE setup time	t_{ALS}[b]	50	–	–	–	–	–	ns
IP_PFLASH_ALE hold time	t_{ALH}	20	–	–	–	–	–	ns
Data setup time	t_{DS}[b]	40	–	–	–	–	–	ns
Data hold time	t_{DH}	20	–	–	–	–	–	ns
Write cycle time	t_{WC}	30	–	–	–	–	–	ns
IP_PFLASH_WE_N high hold time	t_{WH}	15	–	–	–	–	–	ns

a. SDK supports proper register setting for each ONFI Mode.
b. The transition of the corresponding control pins must occur only once while WE is held low.

Table 42: NAND Flash Timing Characteristics

Parameter	Symbol	Min.	Max.	Unit
Ready to IP_PFLASH_RE_N low	t_{RR}	20	–	ns
IP_PFLASH_WE_N high to busy	t_{WB}	–	100	ns
Read cycle time	t_{RC}	30	–	ns
IP_PFLASH_RE_N access time	t_{REA}	–	20	ns
IP_PFLASH_RE_N high to output Hi?Z	t_{RHZ}	–	100	ns
IP_PFLASH_CE_S_N high to output Hi?Z	t_{CHZ}	–	30	ns
IP_PFLASH_RE_N high to output hold	t_{RHOH}	15	–	ns
IP_PFLASH_CE_S_N high to output hold	t_{COH}	15	–	ns
IP_PFLASH_RE_N high hold time	t_{REH}	10	–	ns
IP_PFLASH_RE_N pulse width	t_{RP}	50	–	ns

NOR Flash Interface Timing

The Parallel NOR Flash interface defaults to support the slower 110 ns speed grade devices upon initial booting from the NOR Flash. These parameters can be modified via software configuration.

Figure 34: Parallel NOR Flash Write Timing

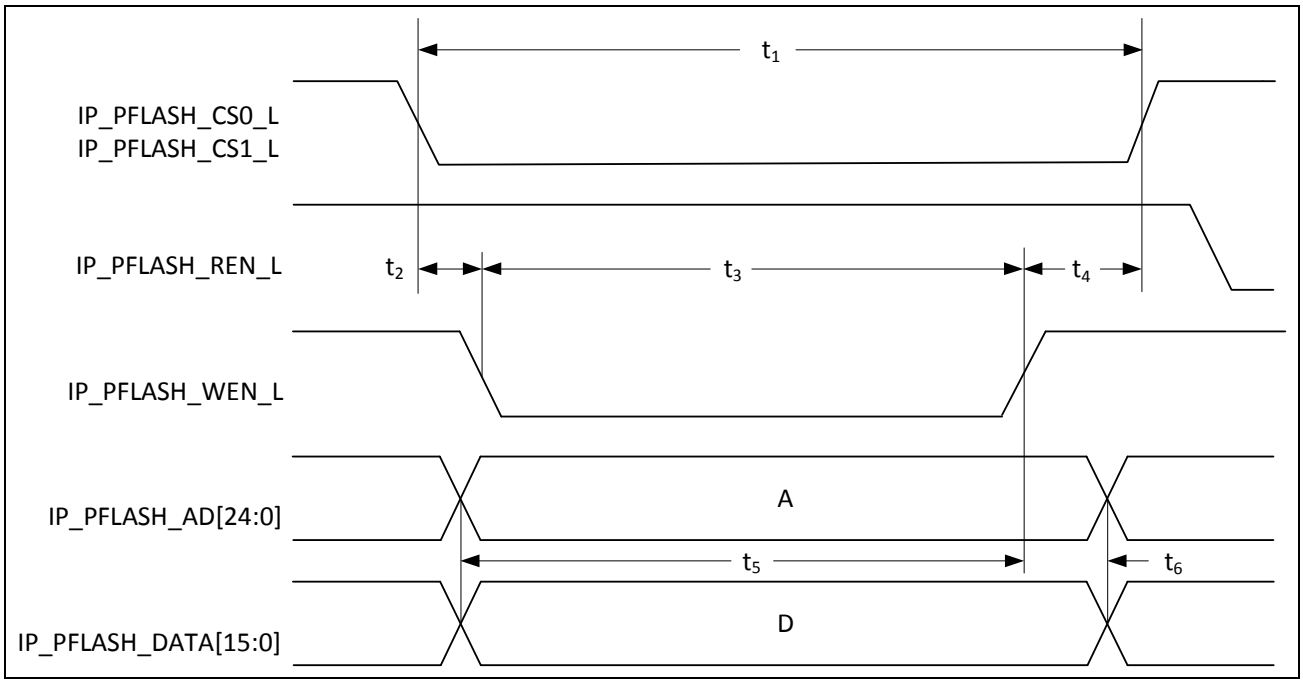


Table 43: Default NOR Flash Write Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
IP_PFLASH_CS[1:0]_L Pulse Width (low)	t_1	–	240	–	ns
IP_PFLASH_WEN_L Assertion Delay After IP_PFLASH_CS[1:0]_L Falling Edge	t_2	–	20	–	ns
IP_PFLASH_WEN_L Pulse Width (low)	t_3	–	120	–	ns
IP_PFLASH_CS[1:0]_L Hold After IP_PFLASH_WEN_L Rising Edge	t_4	–	100	–	ns
IP_PFLASH_AD[24:0], IP_PFLASH_DATA[15:0] Setup to IP_PFLASH_WEN_L Rising Edge	t_5	–	140	–	ns
IP_PFLASH_AD[24:0], IP_PFLASH_DATA[15:0] Hold After IP_PFLASH_WEN_L Rising Edge	t_6	–	100	–	ns

Table 43: Default NOR Flash Write Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Note: For details, see SRAM Cycles Registers PNOR_sram_cycles0_0 and PNOR_sram_cycles0_1 in the Programmer's Register Reference Guide, 5615X5333X_5334X-PR102R **1.** t_1 = t_wcx * 20 **2.** t_2 = 20 **3.** t_3 = t_wpx * 20 **4.** t_4 = (t_wcx - t_wpx - 1) * 20 **5.** t_5 = (t_wpx + 1) * 20 **6.** t_6 = (t_wcx - t_wpx - 1) * 20					

Figure 35: Parallel NOR Flash Read Timing

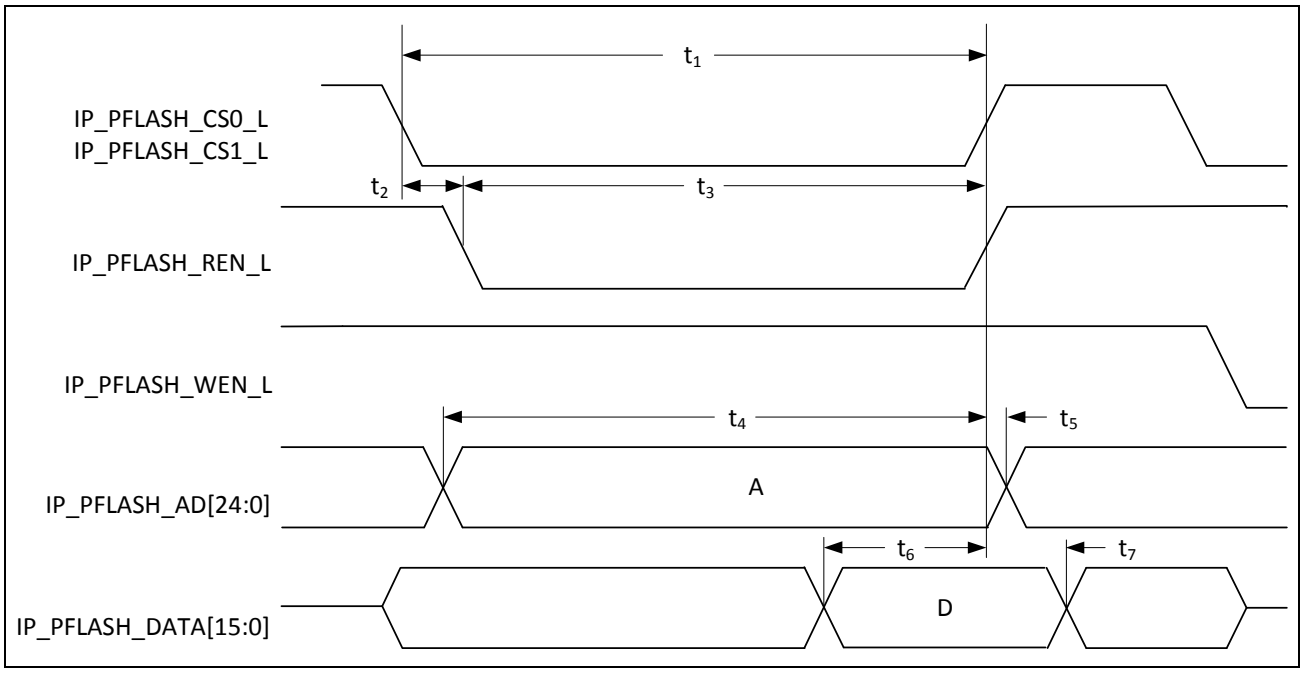


Table 44: Default NOR Flash Read Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
IP_PFLASH_CS[1:0]_L Pulse Width (low)	t_1	–	240	–	ns
IP_PFLASH_REN_L Assertion Delay After IP_PFLASH_CS[1:0]_L Falling Edge	t_2	–	60	–	ns
IP_PFLASH_REN_L Pulse Width (low)	t_3	–	240	–	ns
IP_PFLASH_AD[24:0] Setup to IP_PFLASH_CS[1:0]_L or IP_PFLASH_REN_L Rising Edge	t_4	–	300	–	ns

Table 44: Default NOR Flash Read Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
IP_PFLASH_AD[24:0] Hold After IP_PFLASH_CS[1:0]_L or IP_PFLASH_REN_L Rising Edge	t_5	–	0	–	ns
IP_PFLASH_DATA[15:0] Setup to IP_PFLASH_CS[1:0]_L or IP_PFLASH_REN_L Rising Edge	t_6	20	–	–	ns
IP_PFLASH_DATA[15:0] Hold After IP_PFLASH_CS[1:0]_L or IP_PFLASH_REN_L Rising Edge	t_7	0	–	–	ns

Note: For details, see SRAM Cycles Registers PNOR_sram_cycles0_0 and PNOR_sram_cycles0_1 in the Programmer's Register Reference Guide, 5615X5333X_5334X-PR102R

1. t_1 = t_rcx * 20
2. t_2 = t_ceoex * 20
3. t_3 = (t_rcx - t_ceoex) * 20
4. t_4 = t_rcx * 20
5. t_5 = 0
6. t_6 = Required by internal chip delay
7. t_7 = Required by internal chip delay

BroadSync Timing

Table 45 and Table 46 show the parameters for BroadSync timing, Figure 36 and Figure 37 on page 135 show the timing diagrams.

Table 45: BroadSync Input Timing: Slave Mode

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
BS_BIT_CLK Cycle Time	t_{CYC}	500	–	–	ns
BS_BIT_CLK Duty Cycle	t_{HIGH}	40	–	60	ns
BS_TIME_VAL; BS_SYNC Input Setup Time	t_{ISU}	20	–	–	ns
BS_TIME_VAL; BS_SYNC Input Hold Time	t_{IH}	0	–	–	ns

Figure 36: BroadSync Input Timing—Slave Mode

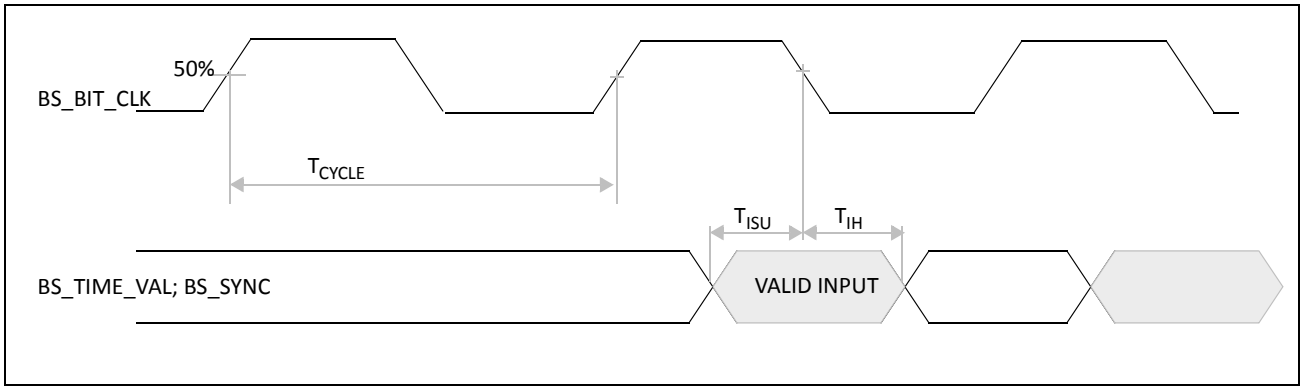
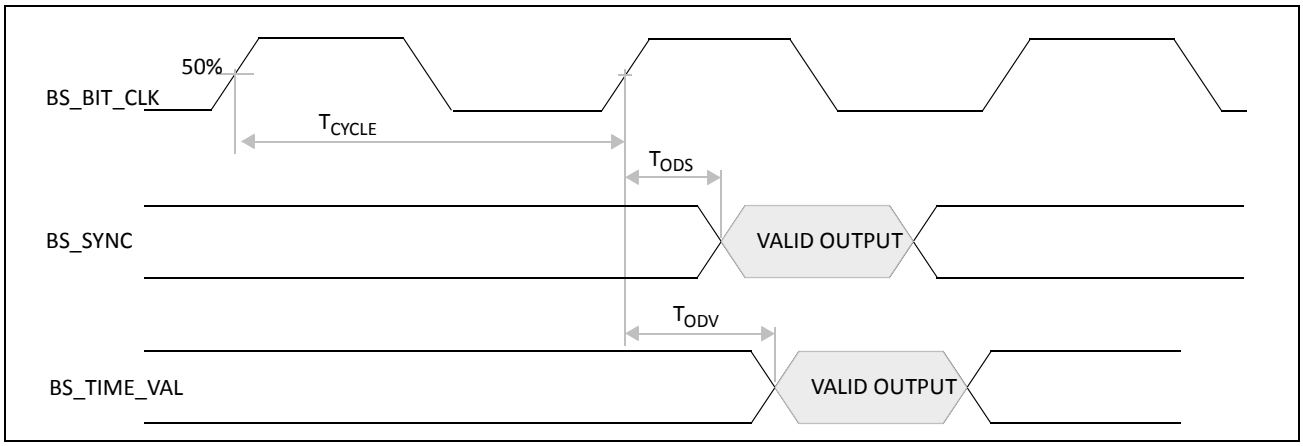


Table 46: BroadSync Output Timing: Master Mode

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
BS_BIT_CLK Cycle Time	t_{CYC}	500	–	–	ns
BS_BIT_CLK Duty Cycle	t_{HIGH}	40	–	60	ns
BS_SYNC Output Delay	t_{ODS}	0	–	20	ns
BS_TIME_VAL Output Delay	t_{ODV}	0	–	20	ns

Figure 37: BroadSync Output Timing—Master Mode



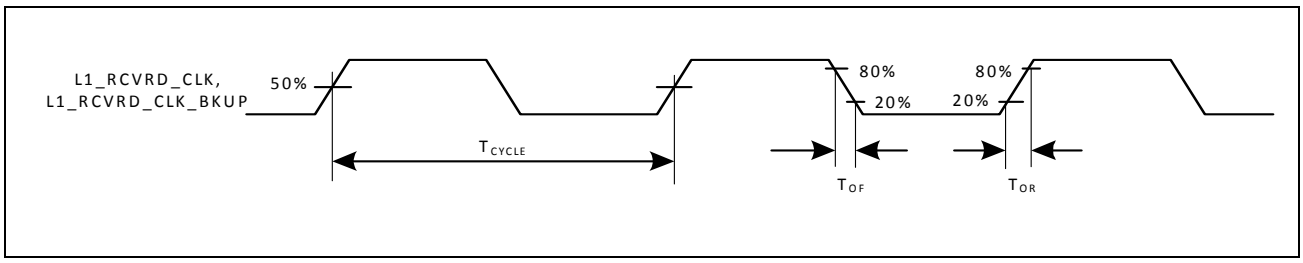
Synchronous Ethernet Interface Timing

L1_RCVRD_CLK and L1_RCVRD_CLK_BKUP Output Timing

Table 47: L1_RCVRD_CLK and L1_RCVRD_CLK_BKUP Output Timing

Parameter	Symbol	Min.	Typ.	Max.	Units
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP Cycle Time	T_{CYCLE}	6.4	–	40	ns
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP Duty Cycle	T_{HIGH}	45	–	55	%
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP Jitter RMS Max (12 kHz to 20 MHz)	–	–	–	60	ps
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP Rise Time from 20% to 80%	T_{OR}	–	–	–	ns
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP Fall Time from 20% to 80%	T_{OF}	–	–	–	ns

Figure 38: Synchronous Ethernet Output Timing Diagram



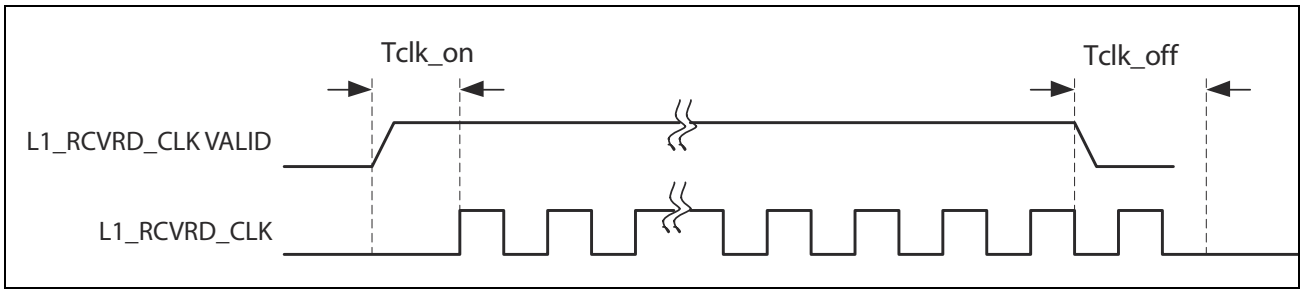
L1_RCVRD_CLK_VALID and L1_RCVRD_CLK Output Timing

The L1_RCVRD_CLK and L1_RCVRD_CLK_VALID timing diagram is shown in Figure 39 on page 137. The L1_RCVRD_CLK_BKUP and L1_RCVRD_CLK_BKUP_VALID timing diagram is similar to the L1_RCVRD_CLK and L1_RCVRD_CLK_VALID signals.

Table 48: L1_RCVRD_CLK_VALID AND L1_RCVRD_CLK Output Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
L1_RCVRD_CLK_VALID TO L1_RCVRD_CLK On Time	T_{CLK_ON0}	0.35	–	1.0	ns
L1_RCVRD_CLK_VALID TO L1_RCVRD_CLK Off Time	T_{CLK_OFF0}	0.35	–	1.0	ns
L1_RCVRD_CLK_BKUP_VALID TO L1_RCVRD_CLK_BKUP On Time	T_{CLK_ON1}	0.35	–	1.0	ns
L1_RCVRD_CLK_BKUP_VALID TO L1_RCVRD_CLK_BKUP Off Time	T_{CLK_OFF1}	0.35	–	1.0	ns

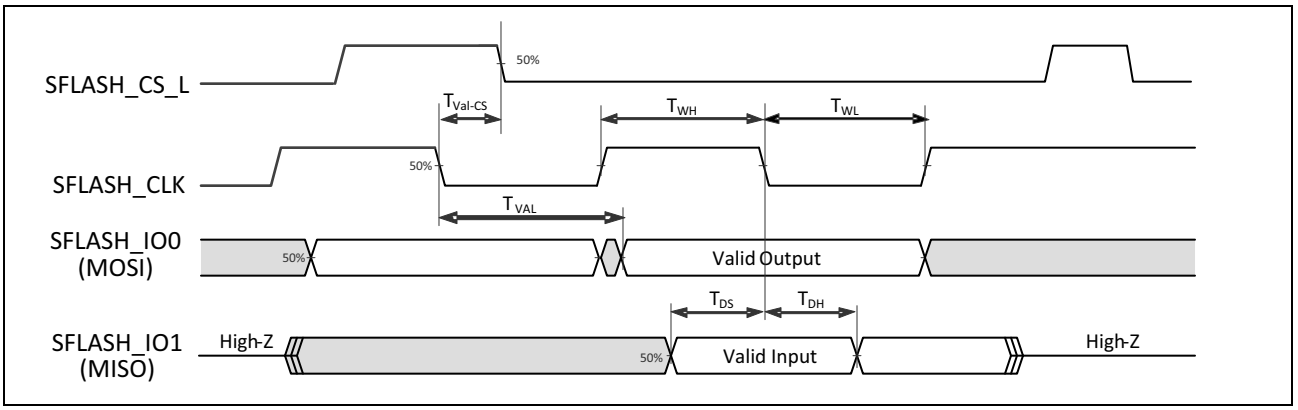
Figure 39: Synchronous Ethernet Interface Timing Diagram



QSPI Flash Interface Timing

The QSPI interface operates as a Master, allowing access to an external SPI Flash or EEPROM from which the microcontroller boot code can be loaded. The SFLASH_CLK, SFLASH_CS_L and SFLASH_IO0 signals are outputs, while SFLASH_IO1 is an input.

Figure 40: QSPI BSPI Mode Master Interface Timing



Note: Figure 40 BSPI Mode only shows single lane operation. SFLASH_IO2 and SFLASH_IO3 signals are used to support dual-lane and quad-lane operation.

Table 49: QSPI BSPI Mode Master Interface Timing Specifications

Parameters	*Symbol*	*Conditions*	*Min.*	*Typ.*	*Max.*	*Unit*
SFLASH Clock Frequency[a]	F_{CLK}	–	–	62.5	62.5	MHz
SFLASH Clock Cycle Time	T_{CK}	–	–	$1/F_{CLK}$	–	ns
SFLASH_CLK Clock High time	T_{WH}	–	$0.4*T_{CK}$	–	$0.6*T_{CK}$	ns
SFLASH_CLK Clock Low time	T_{WL}	–	$0.4*T_{CK}$	–	$0.6*T_{CK}$	ns
Chip Select (SFLASH_CS_L) Valid time	T_{Val-CS}	–	0	–	4.0	ns
Data Out MOSI (SFLASH_IO0) Valid time	T_{Val}	–	–3.0	–	4.0	ns

Table 49: QSPI BSPI Mode Master Interface Timing Specifications (Cont.)

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data In MISO (SFLASH_IO1) Setup time	T_{DS}	–	4.0	–	–	ns
Data In MISO (SFLASH_IO1) Hold time	T_{DH}	–	1.0	–	–	ns
Rise Time	T_R	20% to 80%	–	–	1.5	ns
Fall Time	T_F	20% to 80%	–	–	1.5	ns

a. QSPI BSPI mode is used for initial code download when IP_BOOT_DEV=3'b000 and read operations during runtime. The frequency is set to a reset default value of 25 MHz through CRU_CONTROL.QSPI_CLK_SEL. When register access is established, the same register can be written to change the QSPI interface frequency to a value of 25 MHz, 31.25 MHz, 50 MHz, or 62.5 MHz.

Figure 41: QSPI MSPI Mode Master Interface Timing

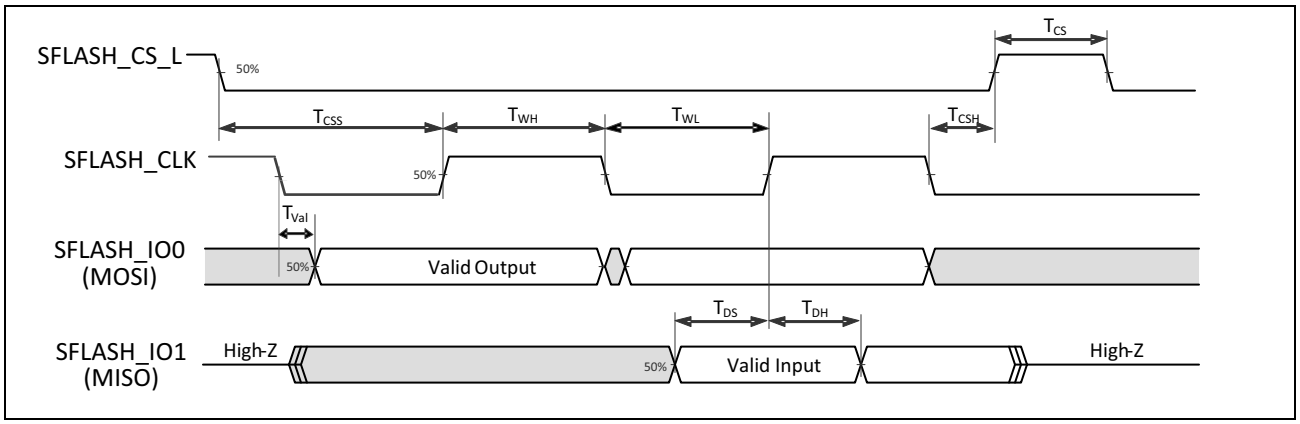


Table 50: QSPI MSPI Mode Master Interface Timing Specifications

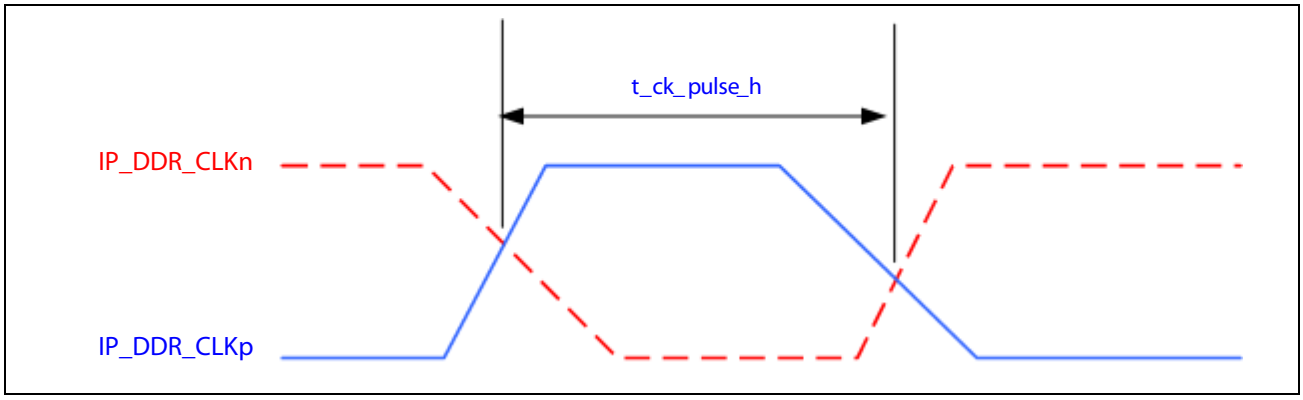
Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
SFLASH Clock Frequency[a]	F_{CLK}	–	–	15.625	15.625	MHz
SFLASH Clock Cycle Time	T_{CK}	–	–	$1/F_{CLK}$	–	ns
SFLASH_CLK Clock High time	T_{WH}	–	$0.4*T_{CK}$	–	$0.6*T_{CK}$	ns
SFLASH_CLK Clock Low time	T_{WL}	–	$0.4*T_{CK}$	–	$0.6*T_{CK}$	ns
Chip Select (SFLASH_CS_L) Setup time	T_{CSS}	–	12.0	–	–	ns
Chip Select (SFLASH_CS_L) Hold time	T_{CSH}	–	1.0	–	–	ns
Data Out MOSI (SFLASH_IO0) Valid time	T_{Val}	–	0	–	4.0	ns
Data In MISO (SFLASH_IO1) Setup time	T_{DS}	–	12.0	–	–	ns
Data In MISO (SFLASH_IO1) Hold time	T_{DH}	–	1.0	–	–	ns
Rise Time	T_R	20% to 80%	–	–	1.5	ns
Fall Time	T_F	20% to 80%	–	–	1.5	ns

a. QSPI MSPI mode is typically used during runtime whenever write or erase operations are required.

DDR3 Interface AC Specifications

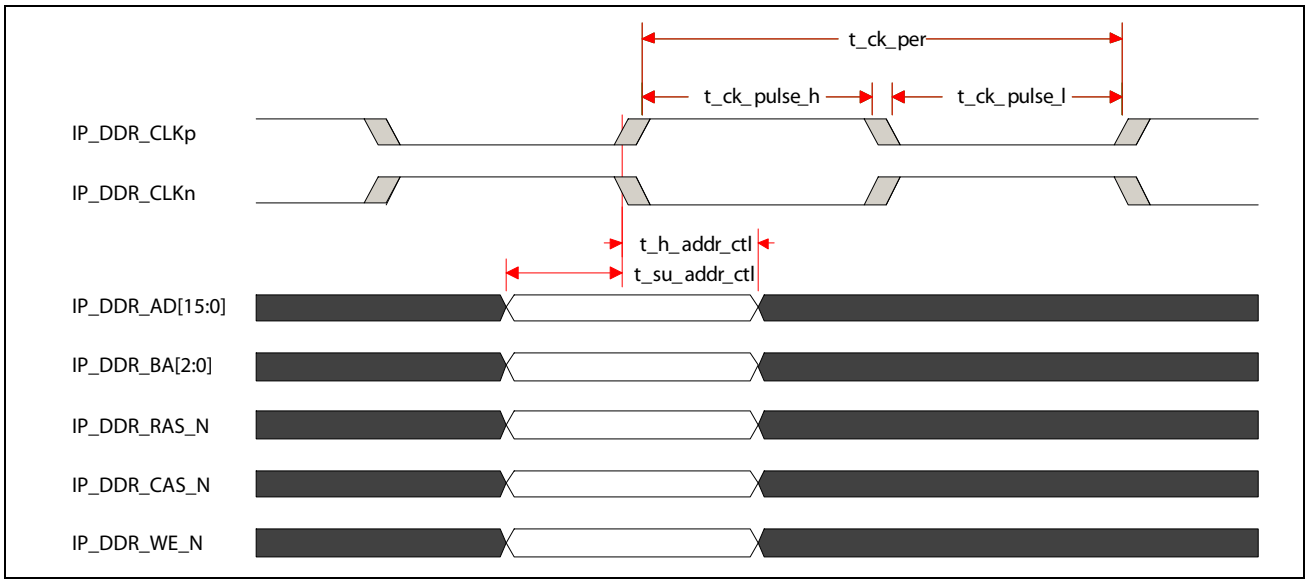
All parameters with respect to IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) are specified relative to the common voltage crossing of the differential pair, as illustrated in Figure 42.

Figure 42: DDR3 CLK Differential Crossing Timing Example



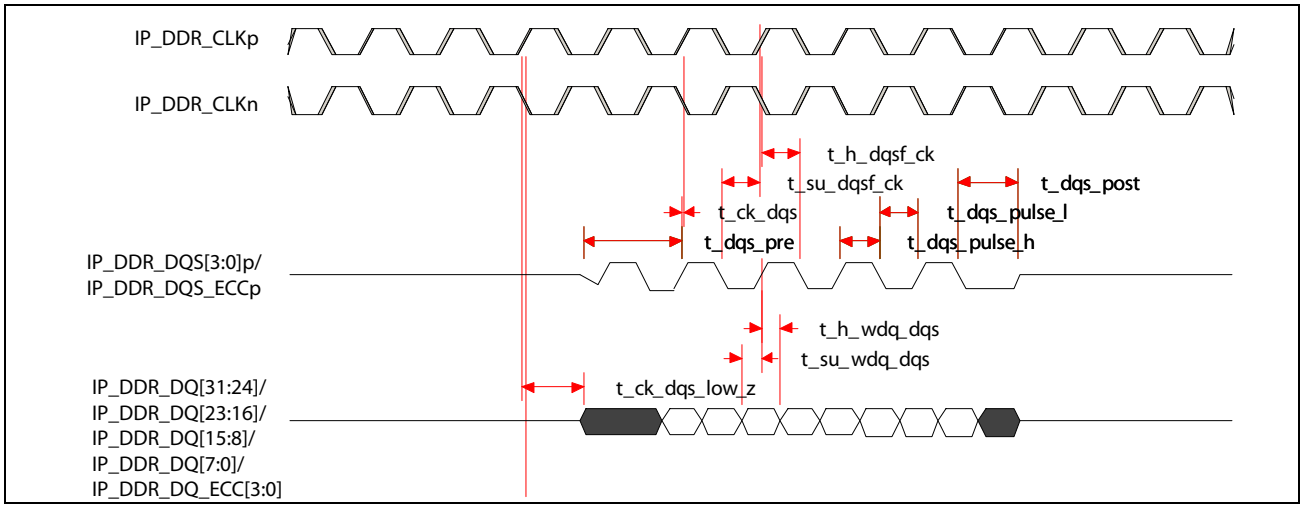
DDR3 Address and Control Timing

Figure 43: DDR3 Address and Control Timing



DDR3 Write Timing

Figure 44: DDR3 Write Timing



DDR3 Read Timing

Figure 45: DDR3 Read Timing

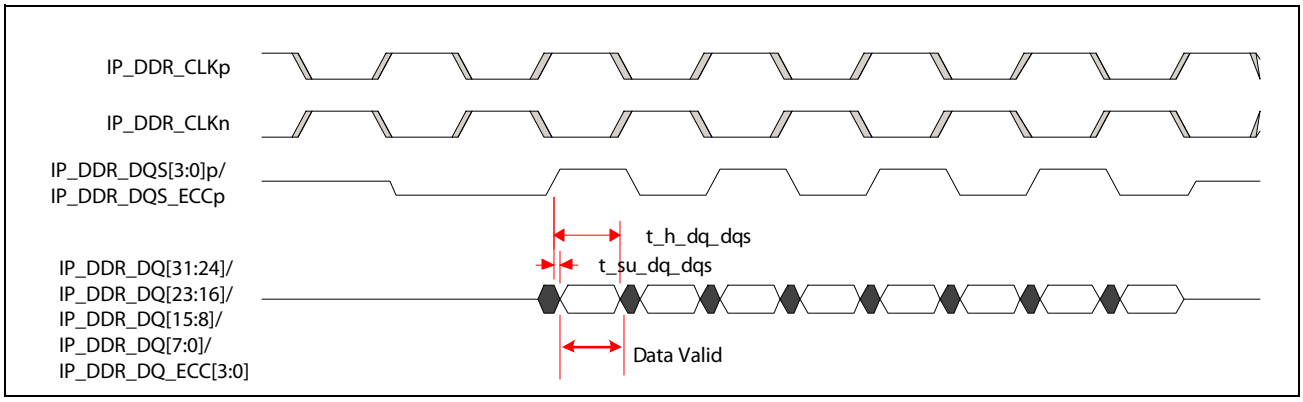


Table 51: AC Specifications for the DDR3-1333 Interface [ab]

Symbol	Parameter [c]	Min[d].	Max.	Unit
Address and Control Timing				
t_ck_jitter	CLK Jitter: IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) cycle-to-cycle jitter	–	±0.080	ns
t_ck_per	CLK Period	1.5	–	ns
t_ck_pulse_h	IP_DDR_CLK_P high (IP_DDR_CLK_N low) minimum pulse width	0.47	0.53	t_ck_per
t_ck_pulse_l	IP_DDR_CLK_P low (IP_DDR_CLK_N high) minimum pulse width	0.47	0.53	t_ck_per

Table 51: AC Specifications for the DDR3-1333 Interface (Cont.)[ab]

Symbol	Parameter [c]	Min[d].	Max.	Unit
t_su_addr_ctl	Address and Control Setup: time that outputs are valid before IP_DDR_CLK_P rising (IP_DDR_CLK_N falling)	190	–	ps
t_h_addr_ctl	Address and Control Hold: time that outputs remain valid after IP_DDR_CLK_P rising (IP_DDR_CLK_N falling)	140	–	ps
Write Timing				
t_ck_dqs	CLK to DQS delay from IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) to IP_DDR_DQS[1:0]_P rising	–0.25	+0.25	t_ck_per
t_su_dqsf_ck	DQS Fall to CLK Rise Setup: delay from IP_DDR_DQS[1:0]_P falling to IP_DDR_CLK_P rising (IP_DDR_CLK_N falling)	0.2	–	t_ck_per
t_h_dqsf_ck	DQS Fall to CLK Rise Hold: delay from IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) to IP_DDR_DQS[1:0]_P falling	0.2	–	t_ck_per
t_dqs_pulse_h	IP_DDR_DQS[1:0]_P high minimum pulse width	0.45	0.55	t_ck_per
t_dqs_pulse_l	IP_DDR_DQS[1:0]_P low minimum pulse width	0.45	0.55	t_ck_per
t_dqs_pre	DQS Preamble: time from tristate-to-low to first rising edge of IP_DDR_DQS[1:0]_P	0.9	–	t_ck_per
t_dqs_post	DQS Postamble: time from last falling edge of IP_DDR_DQS[1:0]_P to tristate	0.3	–	t_ck_per
t_dq_pulse	IP_DDR_DQ[15:0] minimum data valid width	400	–	ps
t_su_wdq_dqs	DQ to DQS Write Setup: time from IP_DDR_DQ[15:8]/IP_DDR_DQ[7:0] output valid to rising or falling edge of IP_DDR_DQS[1:0]_P	30	–	ps
t_h_wdq_dqs	DQ to DQS Write Hold: time IP_DDR_DQ[15:8]/ IP_DDR_DQ[7:0] remains valid after rising or falling edge of IP_DDR_DQS[1:0]_P	65	–	ps
t_ck_dqs_low_z	CLK to DQS LowZ: time from IP_DDR_CLK_P rising (IP_DDR_CLK_N falling) to IP_DDR_DQS[1:0]_P tristate-to-low-z	–500	250	ps

Table 51: AC Specifications for the DDR3-1333 Interface (Cont.)[ab]

Symbol	Parameter [c]	Min[d].	Max.	Unit
Read Timing				
t_su_dq_dqs	DQ to DQS Read Setup[e]: time that IP_DDR_DQ[15:8]/IP_DDR_DQ[7:0] must be valid before the rising or falling edge of IP_DDR_DQS[1:0]_P	NA	–	ps
t_h_dq_dqs	DQ to DQS Read Hold: time that IP_DDR_DQ[15:8]/ IP_DDR_DQ[7:0] must remain valid after the rising or falling edge of IP_DDR_DQS[1:0]_P	0.3	–	t_ck_per

a. All values in the table reflect 50% voltage level timing. Timing shown with 1/4 cycle vdl settings at 667 MHz.
b. All the input signals must meet electrical specifications i.e VIH/VIL & SR specifications.
c. All values in the table reflect Static Timing Analysis (STA) constraints.
d. All STA outputs were timed into a 5 pF standard load.
e. DQ and DQS are nominally aligned. The DQS signal is internally delayed to sample relevant DQ data at the middle of the valid DQ window.

PCIe Interface Timing

PCIE_REFCLK Timing

Figure 46: PCIE_REFCLK Timing

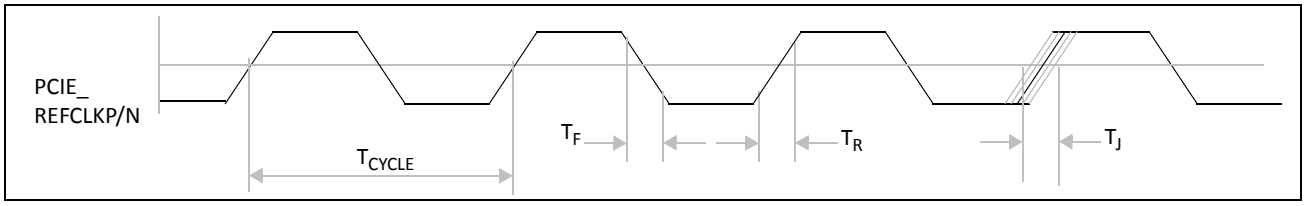


Table 52: PCIE_REFCLK (HCSL)

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Frequency ($1/T_{CYCLE}$)	FREQ	–	100	–	MHz
Tolerance	TOL	–50	–	+50	ppm
Amplitude (Differential pk-pk)	VID	0.30	–	1.7	Vp-p
Duty Cycle	T_h/T_l	40	50	60	%
Rise/Fall Time	T_R/T_F	0.10	–	1.0	ns
Jitter RMS Max (10 kHz–1.5 MHz) for Gen2 5.0 Gbps Operation	T_J	–	–	3.0	ps
Cycle-to-Cycle Jitter for Gen1 2.5 Gbps Operation	–	–	–	150	ps

Note:

- AC-coupled externally.
- Internal termination.
- Series and pull-down termination externally.
- VIH HCSL 660 min 850 max mV (Single ended)
- VIL HCSL -150 min 0 max mV (Single ended)

PCIe_RX Timing

Figure 47: PCIe_RX Timing

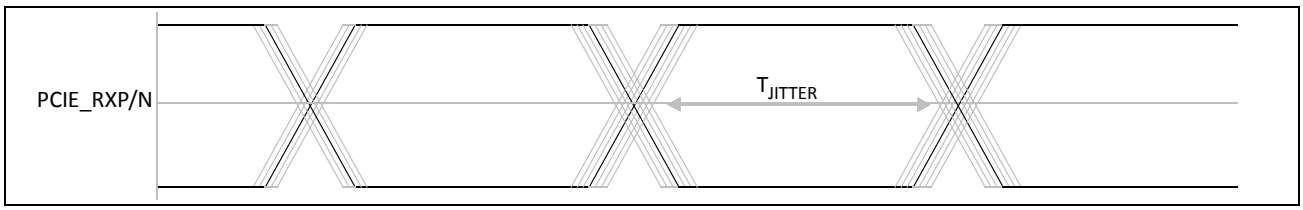


Table 53: PCIe_RX

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Baud Rate	FREQ	–	2.5 or 5.0	–	Gbaud
Input Impedance (Differential)	RIN	80	100	120	Ω
Input Voltage (Differential pk-pk)	VID	175	–	1200	mVp-p
Jitter Tolerance (Min Rx EYE width)	T_J	0.4	–	–	UI

PCIe_TX Timing

Figure 48: PCIe_TX Timing

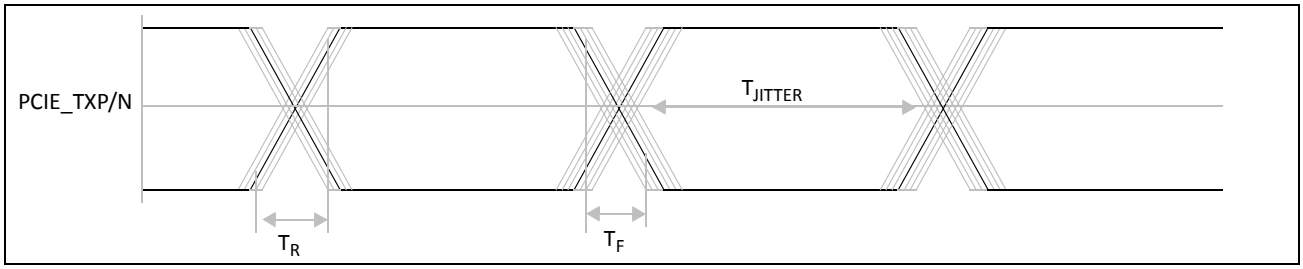


Table 54: PCIe_TX

Parameters	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Units*
Baud Rate	FREQ	–	–	2.5 or 5.0	–	Gbaud
Output Impedance (Differential)	R_{OUT}	–	–	100	120	Ω
Output Voltage (Differential pk-pk)	V_{OD}	–	800	1000	1200	mVp-p
Output Rise/Fall Time (20%–80%)	T_R/T_F	–	0.125	–	–	UI
Output De-Emphasis[a]	V_{OEQ}	Gen1 2.5 Gbps	–3.0	–3.5	–4.0	dB
		Gen1 5.0 Gbps	–5.5	–6.0	–6.5	
Rise/Fall Time (20%–80%)	T_R/T_F	Gen1 2.5 Gbps	0.125	–	–	UI
		Gen1 5.0 Gbps	0.150	–	–	
Jitter (min Tx EYE width)	T_J	–	0.7	–	–	UI

a. Output Deemphasis figures listed in this table are the default settings. TX Deemphasis can be software configured in the range of 0–8 dB, overriding the defaults.

LED Controller Interface

LED_CLK and LED_DATA are outputs. LED_CLK output clock period is 200 ns (5.0 MHz).

Figure 49: LED Timing Diagram

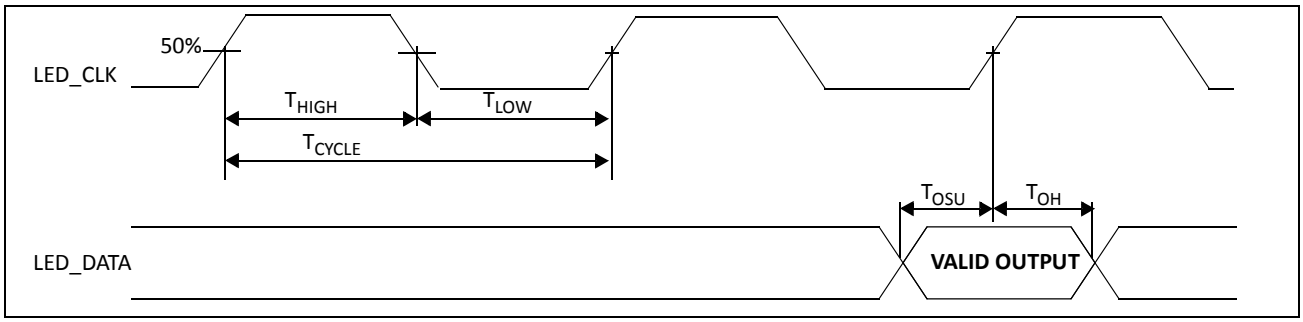


Table 55: LED Timing[a]

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
LED_CLK Cycle Time	T_{CYCLE}	–	200	200	ns
LED_CLK High Time	T_{HIGH}	70	100	130	ns
LED_CLK Low Time	T_{LOW}	70	100	130	ns
LED_DATA Output Valid Time	T_{OV}	0	–	30	ns

a. Timing figures are specified at the 50% crossing thresholds.

XTAL Clock Requirements

The Master clock (XTALP/XTALN), when driven by an external oscillator, requires a 25 MHz single-ended or differential source with characteristics shown in Figure 50 and meets requirements outlined in Table 56.

Figure 50: XTALP/XTALN Input Timing Diagram

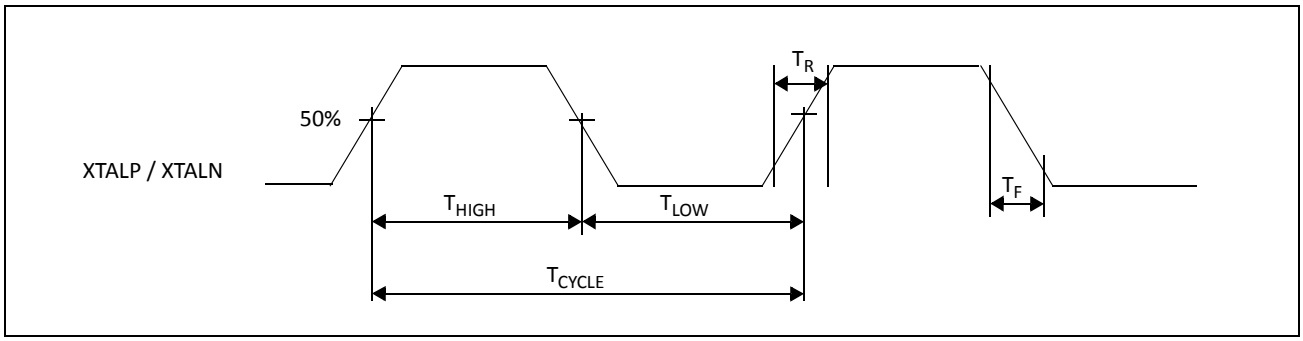


Table 56: XTALP/XTALN Input Requirements

Requirement	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
XTALP/XTALN Frequency	–	–	25	–	MHz
XTALP/XTALN Accuracy	–	–50	–	+50	ppm
XTALP/XTALN Duty Cycle	–	45	–	55	%
Input Voltage Range	VIN	800	–	2000	mVpp diff
Minimum Input Voltage	V_{IL}	0	–	–	V
Maximum Input Voltage	V_{IH}	–	–	1.0	VDC
XTALP/XTALN Rise/Fall Time (20% to 80%)	$T_{R,}$ T_F	0.10	–	1.0	ns
XTALP/XTALN Jitter RMS Max (12 kHz to 12.5 MHz)	–	–	–	0.5	ps

Note:

- Sample part Vectron VCC6-QAB-25M00 LVPECL Crystal Oscillator.
- AC-coupled externally.
- External 100Ω termination required.

XG_PLL2_REFCLK Clock Requirements

The XG oscillator clock (XG_PLL2_REFCLKP/N) requires a 25 MHz differential source with characteristics shown in Figure 51.

Figure 51: XG_PLL2_REFCLKP/N Input Timing Diagram

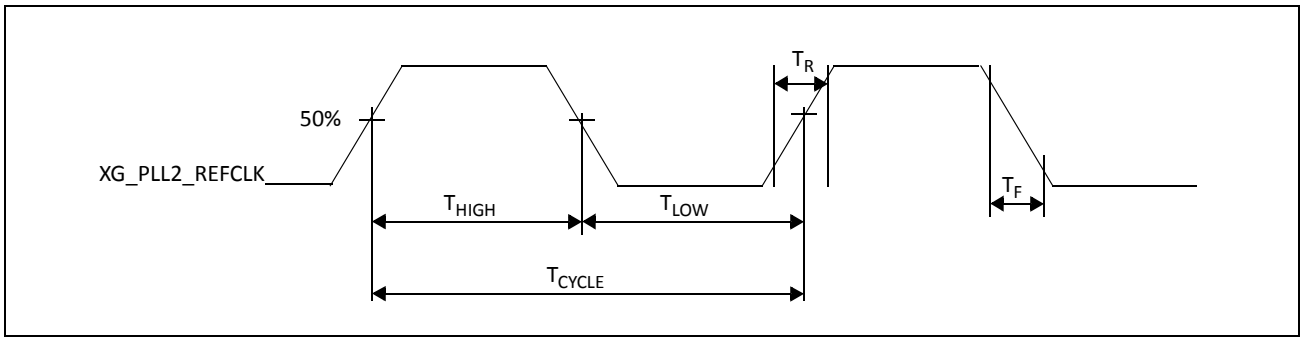


Table 57: XG_PLL2_REFCLK Input Requirements

Requirement	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
XG_PLL2_REFCLK Frequency	–	–	25	–	MHz
XG_PLL2_REFCLK Accuracy	–	–50	–	+50	ppm
XG_PLL2_REFCLK Duty Cycle	–	45	–	55	%
Input Voltage Range	VIN	700	–	2000	mVpp diff
XG_PLL2_REFCLK Rise/Fall Time (20% to 80%)	T_R, T_F	0.10	–	1.0	ns
XG_PLL2_REFCLK Jitter RMS Max (12 kHz to 12.5 MHz)	–	–	–	1.0	ps

Note:

- Sample part Vectron VCC6-QAB-25M00 LVPECL crystal oscillator.
- AC-coupled externally.
- Internal 100Ω termination.

BS[1:0]_PLL_REFCLK Clock Requirements

The BroadSync clocks (BS[1:0]_PLL_REFCLKP/N) requires either a 12.8 MHz, 20 MHz, 25 MHz, or 32 MHz differential source with characteristics shown in Figure 52.

Figure 52: BS[1:0]_PLL_REFCLKP/N Input Timing Diagram

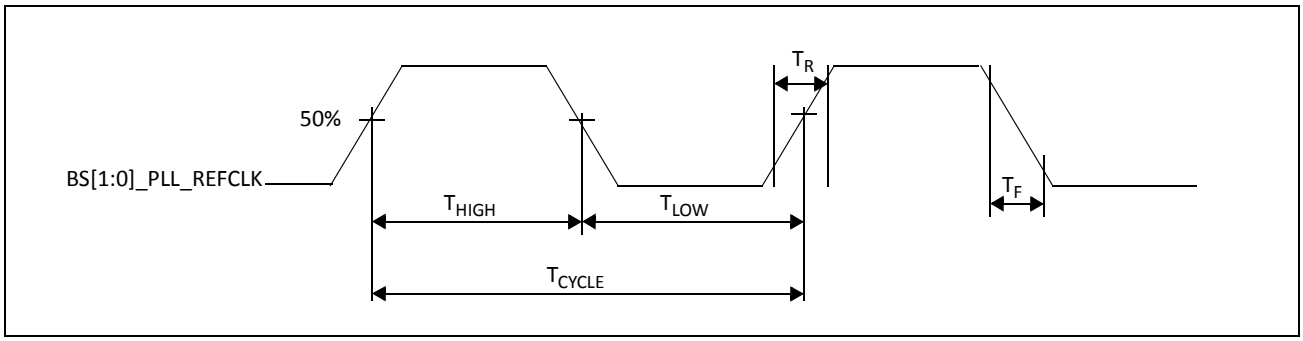


Table 58: BS[1:0]_PLL_REFCLK Input Requirements

Requirement	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
BS[1:0]_PLL_REFCLK Frequency	–	–	(12.8, 20, 25, or 32)	–	MHz
BS[1:0]_PLL_REFCLK Accuracy	–	–50	–	+50	ppm
BS[1:0]_PLL_REFCLK Duty Cycle	–	40	–	60	%
Input Voltage Range	VIN	700	–	2000	mVpp diff
BS[1:0]_PLL_REFCLK Rise/Fall Time (20% to 80%)	T_R, T_F	0.10	–	1.0	ns
BS[1:0]_PLL_REFCLK Jitter RMS Max (12 kHz to 12.5 MHz) is depended upon the requirement of the external driven device.	–	–	–	0.5	ps

Note:

- Sample part Vectron VCC6-QAB-25M00 LVPECL Crystal Oscillator.
- AC-coupled externally.
- Internal 100Ω termination.

TS_PLL_REFCLK Clock Requirements

The TS clock (TS_PLL_REFCLKP/N) requires either a 12.8 MHz, 20 MHz, 25 MHz, or 32 MHz differential source with characteristics shown in Figure 53.

Figure 53: TS_PLL_REFCLKP/N Input Timing Diagram

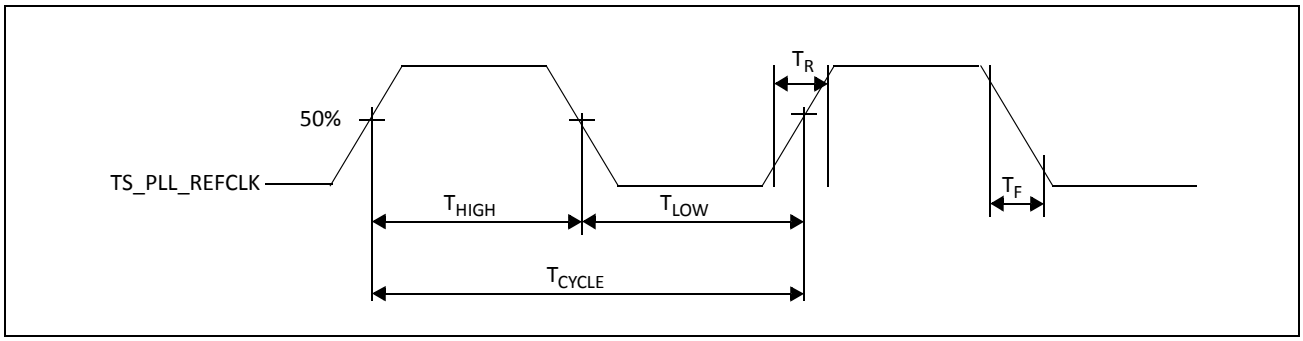


Table 59: TS_PLL_REFCLK Input Requirements

Requirement	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
TS_PLL_REFCLK Frequency	–	–	(12.8, 20, 25, or 32)	–	MHz
TS_PLL_REFCLK Accuracy	–	–50	–	+50	ppm
TS_PLL_REFCLK Duty Cycle	–	40	–	60	%
Input Voltage Range	VIN	500	–	2000	mVpp diff
TS_PLL_REFCLK Rise/Fall Time (20% to 80%)	T_R, T_F	0.10	–	1.0	ns
TS_PLL_REFCLK Jitter RMS Max (12 kHz to 12.5 MHz)	–	–	–	2.0	ps

Note:

- Sample part Rakon Limited® P5473LF (OCXO) crystal oscillator.
- AC-coupled externally.
- Internal 100Ω termination.

LC_PLL1_REFCLK Clock Requirements

The Warpcore Technology clocks (LC_PLL1_REFCLKP/N) each require either a 25 MHz or 156.25 MHz differential source with characteristics shown in Figure 54.

Figure 54: LC_PLL1_REFCLKP/N Input Timing Diagram

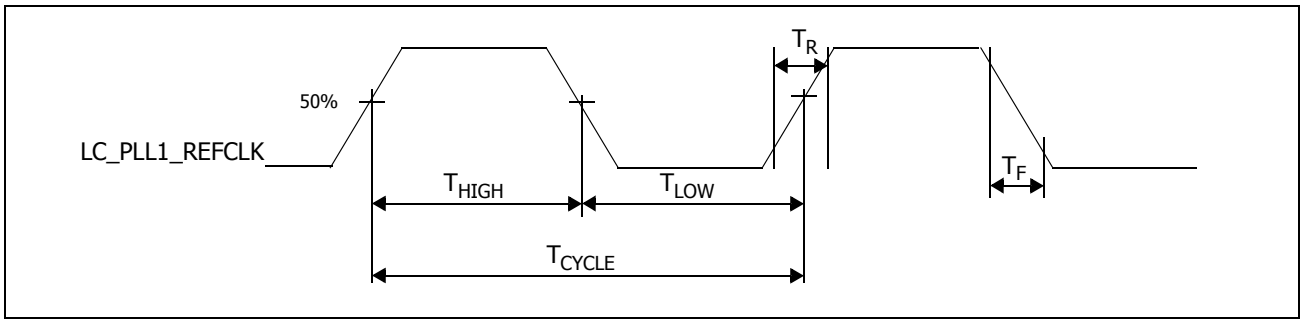


Table 60: LC_PLL1_REFCLK Input Requirements

Requirement	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
LC_PLL1_REFCLK Frequency	–	–	25 or 156.25	–	MHz
LC_PLL1_REFCLK Accuracy	–	–50	–	+50	ppm
LC_PLL1_REFCLK Duty Cycle	–	45	–	55	%
Input Voltage Range	VIN	700	–	2000	mVpp diff
LC_PLL1_REFCLK Rise/Fall Time (20% to 80%)	T_R, T_F	0.10	–	1.0	ns
LC_PLL1_REFCLK (156.25 MHz) Jitter RMS Max (12 kHz to 20 MHz)	–	–	–	0.5	ps
LC_PLL1_REFCLK (25 MHz) Jitter RMS Max (12 kHz to 12.5 MHz)	–	–	–	0.5	ps

Note:

- Sample part Valpey Fisher VF900892-156.25 or Raltron Electronics CS9-TSH-156.250 LVPECL Crystal Oscillator or Vectron VCC6-1286-156M250, or MtronPTI M2013S232 (156.25 MHz).
- AC-coupled externally.
- Internal 100Ω termination.
- Input options: 25 MHz oscillator or 156.25 MHz oscillator.

LC_PLL0_REFCLK Clock Requirements

The QSGMII/QGPHY clock (LC_PLL0_REFCLKP/N) requires a 25 MHz differential source with characteristics shown in Figure 55.

Figure 55: LC_PLL0_REFCLKP/N Input Timing Diagram

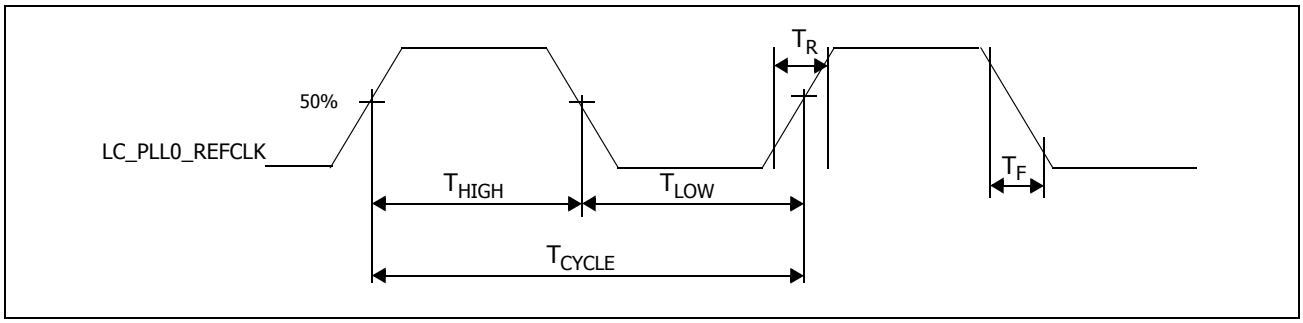


Table 61: LC_PLL0_REFCLK Input Requirements

Requirement	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
LC_PLL0_REFCLK Frequency	–	–	25	–	MHz
LC_PLL0_REFCLK Accuracy	–	–50	–	+50	ppm
LC_PLL0_REFCLK Duty Cycle	–	45	–	55	%
Input Voltage Range	VIN	700	–	2000	mVpp diff
LC_PLL0_REFCLK Rise/Fall Time (20% to 80%)	T_R, T_F	0.10	–	1.0	ns
LC_PLL0_REFCLK (25 MHz) Jitter RMS Max (12 kHz to 12.5 MHz)	–	–	–	0.5	ps

Note:

- AC-coupled externally.
- Internal 100Ω termination.

EXT_QS2_CLKP/N Clock Specifications

These clocks (EXT_QS2_CLKP/N) provide a 125 MHz differential clocks that can be directly connecting to external GPHY such as Broadcom BCM54282.

Figure 56: EXT_QS2_CLKP/N Output Timing Diagram

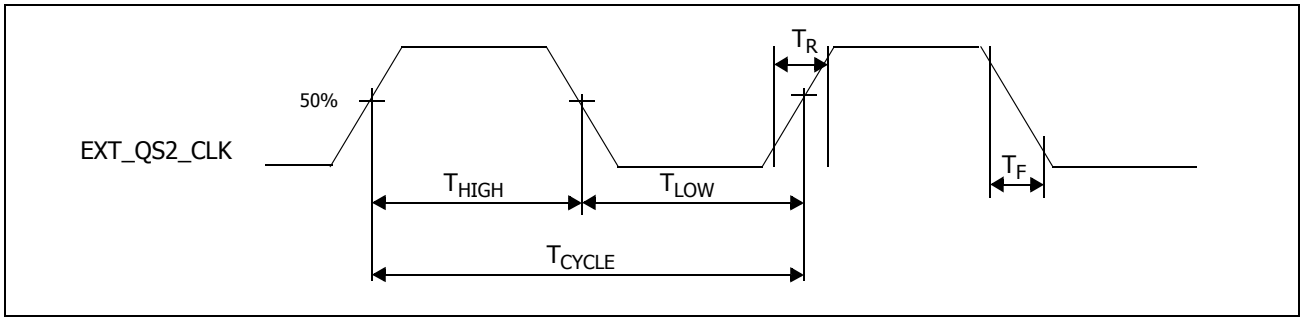


Table 62: EXT_QS2_CLKP/N Output Specifications

Requirement	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
EXT_QS2_CLK Frequency	–	–	125	–	MHz
EXT_QS2_CLK Accuracy	–	–50	–	+50	ppm
EXT_QS2_CLK Duty Cycle	–	45	–	55	%
Output Voltage Range	V_{ODIFF}	300	–	500	mVpp diff
EXT_QS2_CLK Rise/Fall Time (20% to 80%)	$T_{R,}$ T_F	0.10	–	0.22	ns
EXT_QS2_CLK Jitter RMS Max (12 kHz to 20 MHz)	–	–	–	2	ps

Note:

- AC-coupled externally.
- Measured with 50Ω termination as recommended in the Hardware Design Guide.

BS[1:0]_PLL_CLK Clock Specifications

The BroadSync clock outputs (BS[1:0]_PLL_CLKP/N) provide a differential clock source depended upon BS[1:0]_PLL_REFCLKP/N input clock frequencies (20, 25, 125, or 156.25) MHz as shown in Figure 52.

Figure 57: BS[1:0]_PLL_CLKP/N Output Timing Diagram

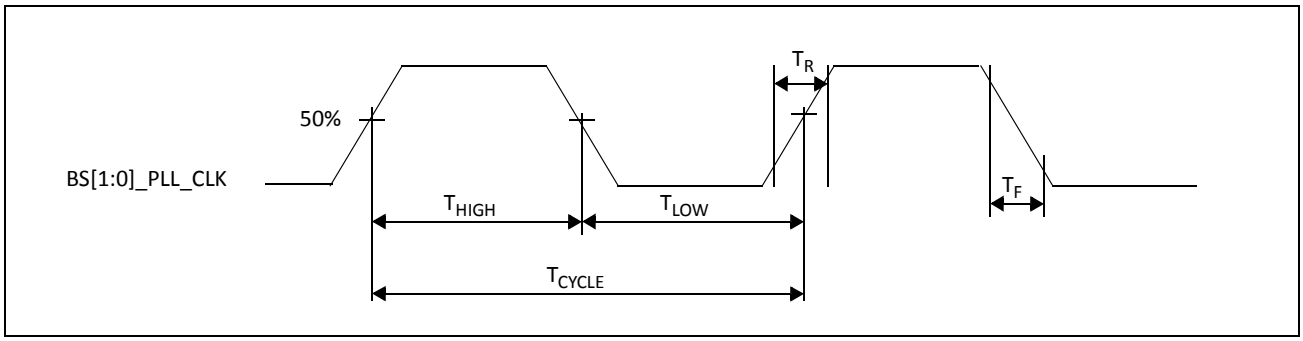


Table 63: BS[1:0]_PLL_CLK Output Specifications

Requirement	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
BS[1:0]_PLL_CLK Frequency	–	–	20, 25, 125, or 156.25	–	MHz
BS[1:0]_PLL_CLK Accuracy	–	–50	–	+50	ppm
BS[1:0]_PLL_CLK Duty Cycle	–	40	–	60	%
Output Voltage Range	V_{ODIFF}	300	–	500	mVpp diff
BS[1:0]_PLL_CLK Rise/Fall Time (20% to 80%)	T_R, T_F	0.10	–	0.22	ns
BS[1:0]_PLL_CLK Jitter RMS Max for 20 MHz	–	15	–	20	ps
25 MHz	–	15	–	20	ps
125 MHz	–	5	–	6	ps
156.25 MHz	–	5	–	6	ps

Note:

- AC-coupled externally.
- Measured with 50Ω termination as recommended in the Hardware Design Guide.

QSGMII AC Specifications

Transmitter

Figure 58: QSGMII Transmit Eye Mask

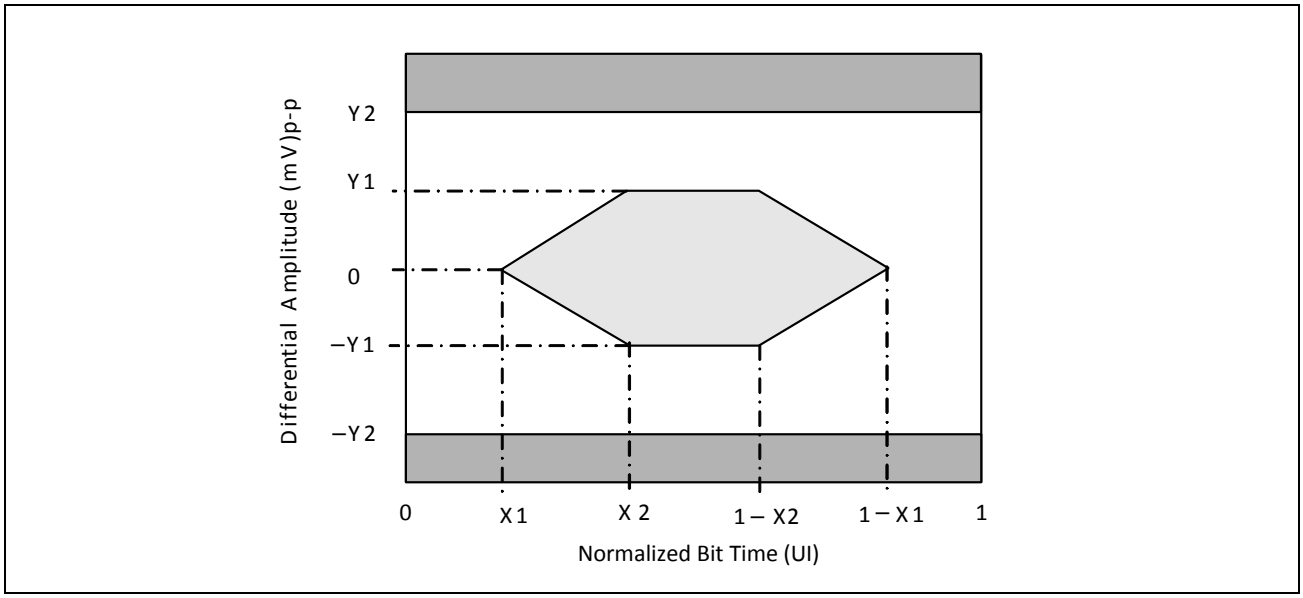


Table 64: QSGMII TX

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Output Speed per lane	–	–100 ppm	+5.0	+100 ppm	Gbaud
Differential Resistance	Rin	80	100	120	Ω
Differential Output Voltage (pk-pk)	VOD	400	–	900	mVp-p
Transmit Eye Mask (Figure 58)	X1	–	–	0.15	UI
Transmit Eye Mask (Figure 58)	X2	–	–	0.40	UI
Transmit Eye Mask (Figure 58)	Y1	200	–	–	mV
Transmit Eye Mask (Figure 58)	Y2	–	–	450	mV
Common Mode Voltage	VCM	550	–	1060	mV
Differential Output Return Loss (min)	Equation[a]	–	–	–8	dB
Common-mode Output Return Loss (min)	Equation[b]	–	–	–6	dB
Output Rise Time (20%–80%)	Tr	30	–	–	pS
Output Fall Time (20%–80%)	Tf	30	–	–	pS
Output Jitter @ $1e^{-12}$ BER					
Uncorrelated	sut	–	–	0.15	UIpp
Total	st	–	–	0.30	UIpp

a. Return Loss (f) –8 dB for 100 MHz ≤ f< 2.5 GHz.
Return Loss (f) ≤ [–8+16.6log(f/2.5)]dB for 2.5 GHz ≤ f ≤ 5 GHz, where f is in Gigahertz.
b. Return Loss (f) ≤ –6 dB for 100 MHz ≤ f < 2.5 GHz.

Receiver

Figure 59: QSGMII Receive Eye Mask

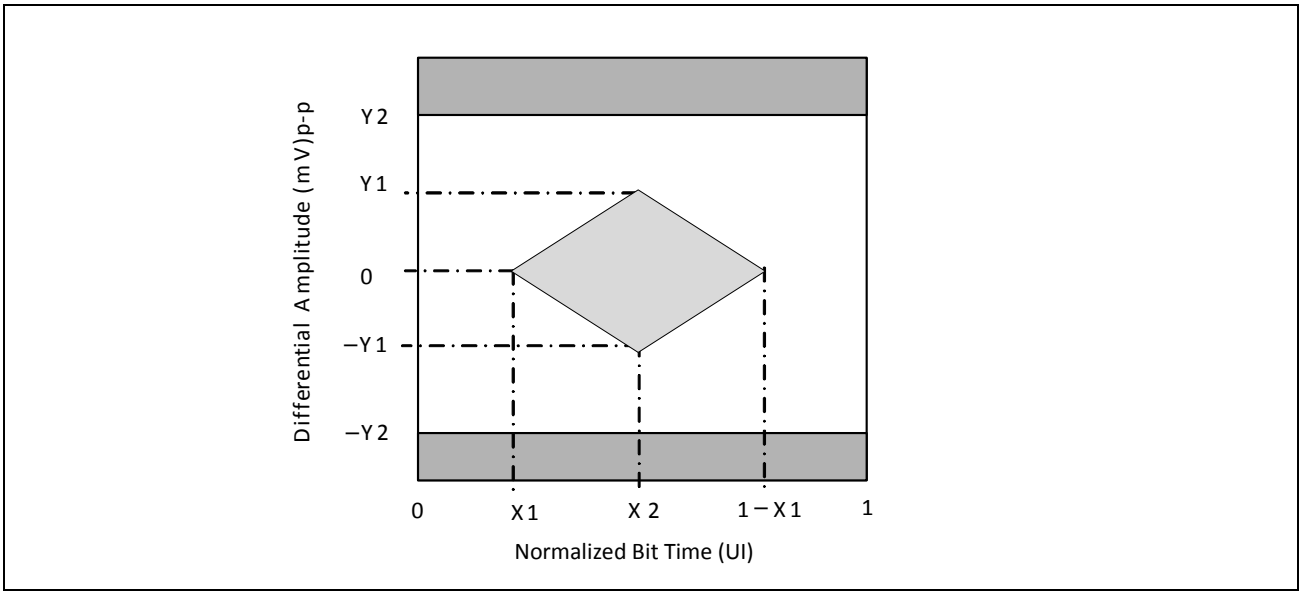
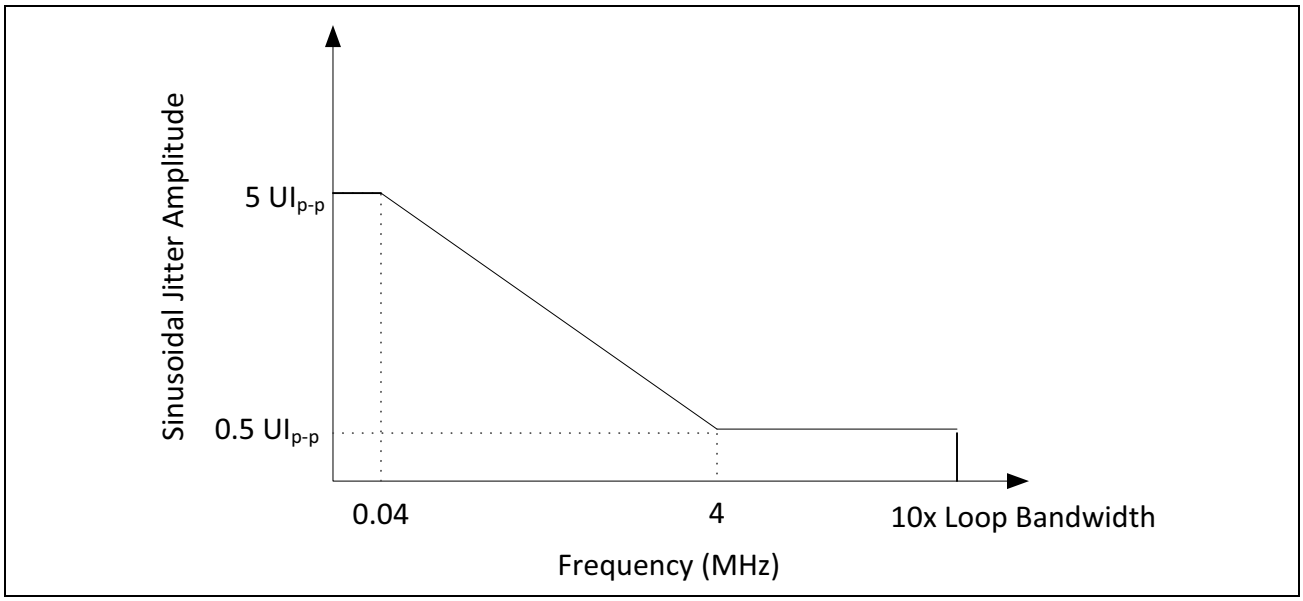


Table 65: QSGMII RX

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Receiver coupling	AC	–	0.1	–	µF
Differential Resistance	Rin	80	100	120	Ω
Receive eye mask (Figure 59 on page 155)	X1	–	–	0.30	UI
Receive eye mask (Figure 59 on page 155)	X2	–	–	0.5	UI
Receive eye mask (Figure 59 on page 155)	Y1	50	–	–	mV
Receive eye mask (Figure 59 on page 155)	Y2	–	–	450	mV
Differential input return loss	Equation[a]		–	–8	dB
Common mode input return loss	Equation[b]		–	–6	dB
Receiving speed per lane	–	–100 ppm	+5.0	+100 ppm	Gbaud
Sinusoidal jitter tolerance	Figure 60 on page 156	–	–	0.05	UIpp
Bit error rate based channel characteristics per Clause 83A in IEEE802.3ba.	–	–	–	1e-12	bps

a. Return loss (f) ≤ –8 dB for 100 MHz ≤ f < 2.5 GHz.
Return loss ≤ [–8 + 16.6log(f/2.5)]dB for 2.5 GHz ≤ f ≤ 5 GHz, where f is in Gigahertz.
b. Return loss (f) ≤ –6 dB for 100 MHz ≤ f < 2.5 GHz, where f is in Gigahertz.

Figure 60: Single-Tone Sinusoidal Jitter Mask



SGMII AC Specifications

This subsection specifies timing information for the Serial Interface.

SGMII/SerDes Interface Output Timing

Figure 61: SGMII Serial Interface Output Timing

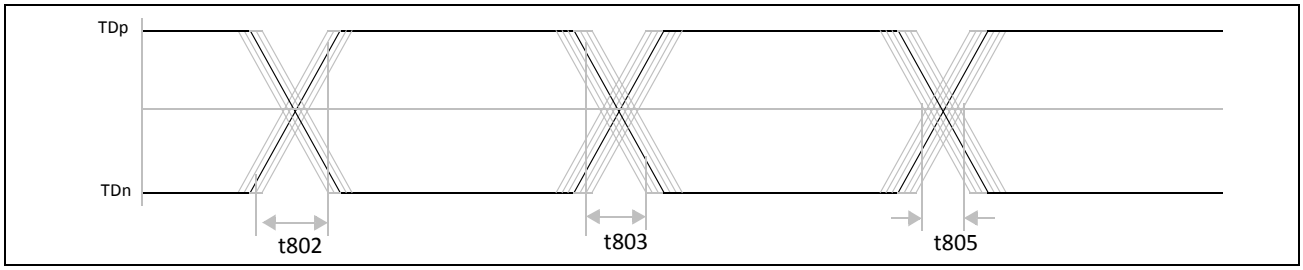


Table 66: SGMII Serial Interface Output Timings

Description	*Parameter*	*Min.*	*Typ.*	*Max.*	*Units*
Transmit Data Signaling Speed	t801	–	1.25	–	Gbaud
Transmit Data Rise Time (20%–80%)	t802	100	–	200	ps
Transmit Data Fall Time (20%–80%)	t803	100	–	200	ps
Transmit Data Total Jitter	t805	–	–	0.24	UI

SGMII/SerDes Interface Input Timing

Figure 62: Serial Interface Input Timing

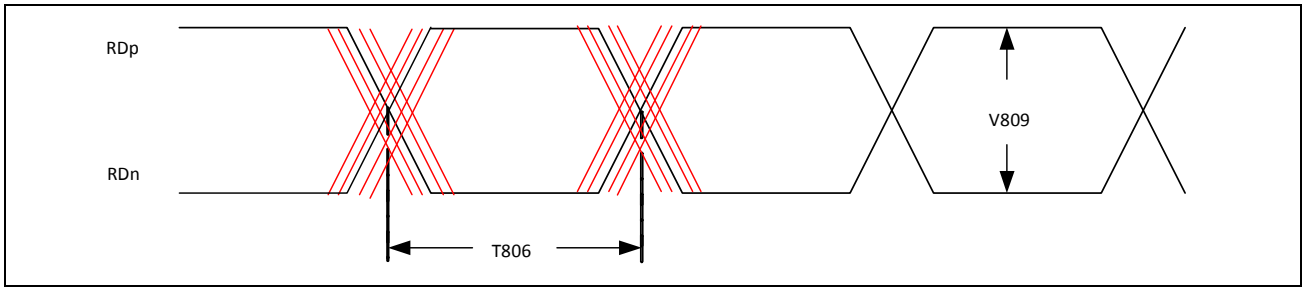


Table 67: SGMII Serial Interface Input Timings

Description	*Parameter*	*Min.*	*Typ.*	*Max.*	*Units*
Receive Data Signaling Speed	t806	–	1.25	–	Gbaud
Receive Data Differential Input (pk-pk)	V809	0.1	–	–	V

2.5GbE SerDes AC Specifications

This subsection specifies timing information for the SerDes Interface running at this rate.

2.5GbE/SerDes Interface Output Timing

Figure 63: 2.5GbE/SerDes Interface Output Timing

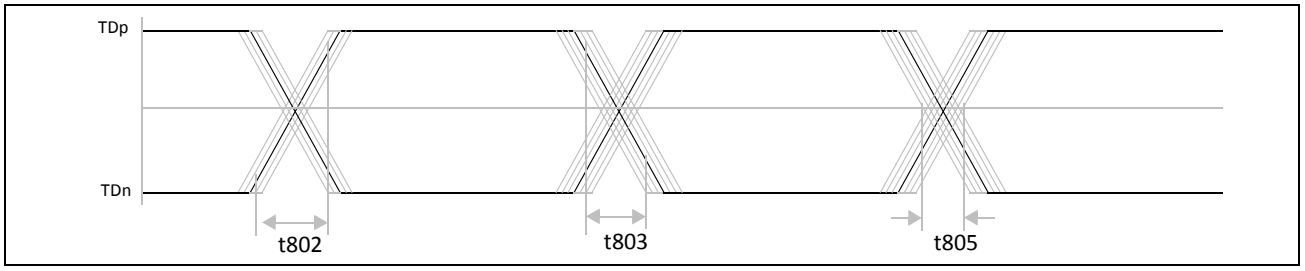


Table 68: 2.5GbE/SerDes Interface Output Timings

Description	*Parameter*	*Min.*	*Typ.*	*Max.*	*Units*
Transmit Data Signaling Speed	t801	–	3.125	–	Gbaud
Transmit Data Rise Time (20%–80%)	t802	60	100	130	ps
Transmit Data Fall Time (20%–80%)	t803	60	–	130	ps
Transmit Data Total Jitter	t805	–	–	0.65	ps
Transmit P to N Differential Skew	T_{SKEW}	–	–	15	ps

2.5GbE/SerDes Interface Input Timing

Figure 64: 2.5GbE/SerDes Interface Input Timing

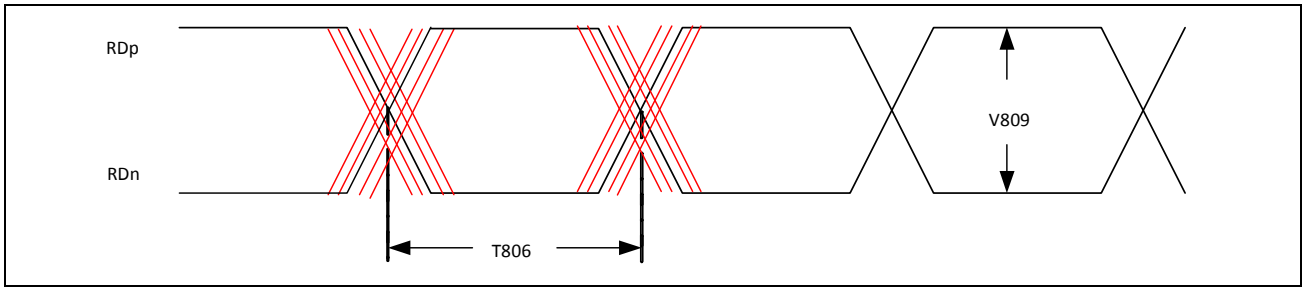


Table 69: 2.5GbE/SerDes Interface Input Timings

Description	*Parameter*	*Min.*	*Typ.*	*Max.*	*Units*
Receive Data Signaling Speed	t806	–	3.125	–	Gbaud
Receive Data Differential Input (pk-pk)	V809	0.1	–	1.6	V

Warpcore Technology Serial Interface AC Specification

The device serial interface supports the following features:

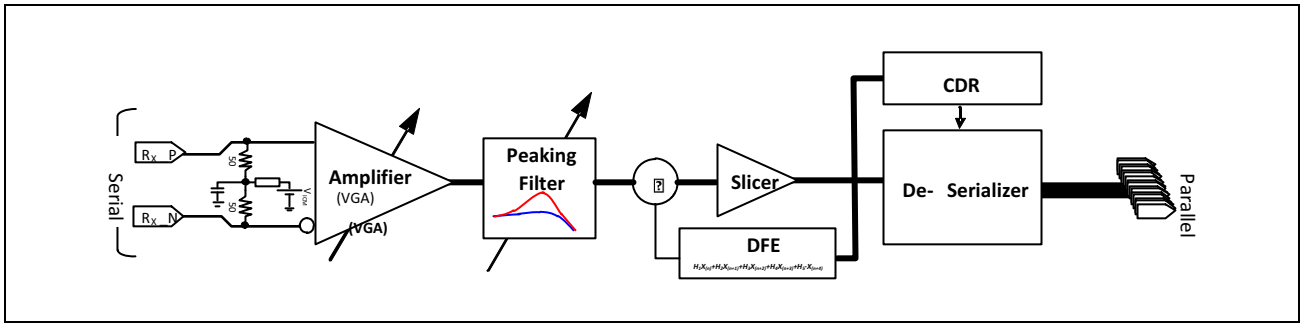
- Quad SerDes block supporting four serial links.
- Support for line rates of 1.25 Gbps, 3.125 Gbps, 5.1625 Gbps, 6.5625 Gbps, 10.3125 Gbps, and 10.9375 Gbps per serial link.
- Includes a 5-tap DFE with adaptive control and VGA with AGC.
- Programmable RX equalizer with 0 dB–8 dB boost, approximately 0.5 dB/step.
- Transmitter with 32-level post-cursor and 16-level precursor preemphasis.
- CML driver with 2 × 50Ω internal termination.
- Controlled peak-to-peak amplitude.
- 4-Tap FIR with configurable weights:
  - 1-Tap of Precurser emphasis (16 steps)
  - 1-Tap of Post-curser emphasis (32 steps)
  - Additional second Post-curser emphasis (8 steps)

The serial interface operating conditions are shown in Table 70.

Table 70: Warpcore Technology Serial Interface Operating Conditions

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Baud, symbol rate	B_{PS}	1.25	–	10.9375	Gbaud
Unit Interval	UI	91.4	–	800	ps

Figure 65: Conceptual Diagram of the SerDes Receiver



The Serial Interface receive characteristics are shown in Table 71.

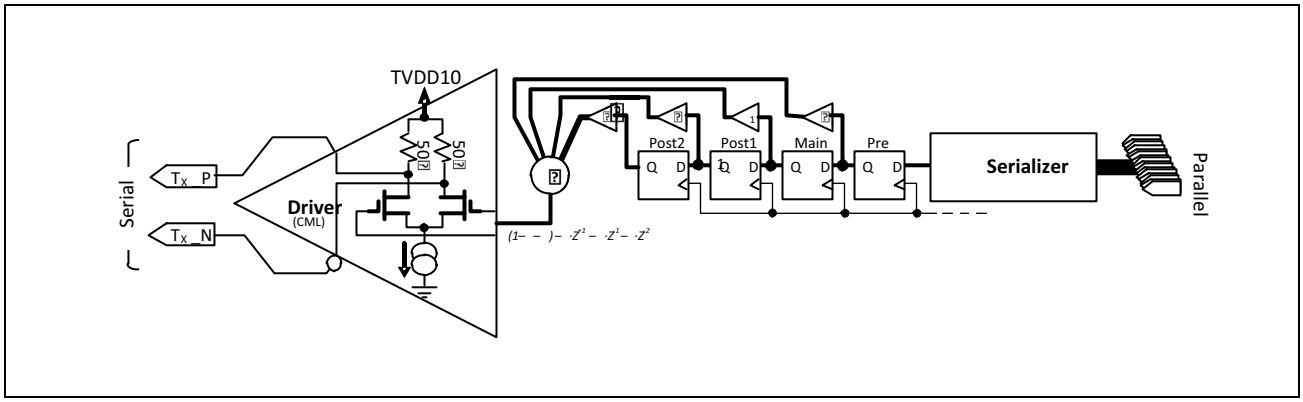
Table 71: Serial Interface Receive Characteristics

Parameter	*Symbol*	*Description*	*Min.*	*Typ.*	*Max.*	*Unit*
Input Voltage	V_{ID}	AC coupled, differential p-p	100	–	1600	mV
Input Referred Offset	V_{OFF}	Data/phase comparator	–	1	–	mV
Input Impedance	R_{in}	Differential, integrated on-chip	80	100	120	Ω
Input Bandwidth	BW_{in}	–3 db level	5	–	–	GHz

Table 71: Serial Interface Receive Characteristics (Cont.)

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Bit Error Rate	BER	–	–	–	10^{-12}	1/s
Jitter Tolerance	delta-t_{RXtot}	Total, peak-peak	–	–	0.65	UI
	delta-t_{RXdet}	Deterministic, peak-peak	–	–	0.37	UI
Input Differential Skew	t_{skewi}	50% rising/falling versus 50% falling/rising edge.	–	–	TBD	UI

Figure 66: Conceptual Diagram of the SerDes Transmitter



The serial interface transmit characteristics are shown in Table 72.

Table 72: Serial Interface Transmit Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Output Voltage	V_{OD}	Differential peak-peak Programmable in 16 steps	0.7	1.0	1.1	Vppd
Preemphasis	alpha	FIR tap coefficient in 32 steps. alpha ~= 0.0125i, where i = 0 ~ 31	0	–	0.3875	–
	beta	FIR tap coefficient in 16 steps. beta ~= 0.0125i, where i = 0 ~ 15	0	–	0.1875	–
	chi	FIR tap coefficient in 8 steps. chi ~= 0.0125i, where i = 0 ~ 7	0	–	0.875	–
Output Impedance	R_{out}	Differential, integrated on-chip	–	100	–	Ω
Output voltage fall-time	t_{fall}	80% to 20% (based on 10GBASE-KR waveform, 8–1s, 8–0s)	24	–	47	ps
Output voltage rise-time	t_{rise}	20% to 80%	24	–	47	ps
Output Differential Skew	t_{skewo}	50% rising/falling versus 50% falling/rising edge	–	–	15	ps

Table 72: Serial Interface Transmit Characteristics (Cont.)

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Transmit Output Jitter	delta-t_{TXWDM}	Total, peak-peak WDM	–	–	TBD	UI
	delta-t_{TXtot}	Total, peak-peak	–	–	0.28	UI
	delta-t_{TXdet}	Deterministic, peak-peak	–	–	0.17	UI

WCx_TDy Transmit Preemphasis Setting

The 4-tap preemphasis FIR has a transfer function of $(1–\alpha–\beta) – \beta z^{+1} – \alpha z^{-1} – X^{z-1}$. The preemphasis level is controllable through tx_ctrl[47:45] for the second post-cursor tap, but unlike previous cores, the pre, main, and post1 taps are directly and independently controlled by the KR, Clause 72 logic. The control bits for these CL72 taps are listed in Table 73, and the LSB size is 0.125 or 2.5%. These bits can be accessed through the Clause 72 registers (such as 0x82E2), and the bit description is 15 – force, 14:10 – post1, 9:4 – main, 3:0 – pre.

Table 73: CL72 Taps

Name	Description Tap	Weight	Percentage	dB
txi_fir_tap_main[5:0]	FIR main tap	0.2125 – 1	21.25% - 100%	–
txi_fir_tap_post[4:0]	FIR post1 tap	0 – 0.3875	0 – 77.5%	0 – -13
txi_fir_tap_pre[3:0]	FIR pre tap	0 – 0.1875	0 – 37.5%	0 – -4
txi_ctrl[47:45]	FIR post2 tap{2:0}	0 – 0.0875	0 – 17.5%	0 – -1.7
Note: For some lower rates, such as 3.125G, pll_ctrl<3> should be set = 1 for proper operation of the FIR.				

To conserve power, it is recommended to add equalization with the RX peaking filter, default value is 4 dB–5 dB, before adding any TX preemphasis.

10GBASE-KR Electrical Characteristics

Transmitter

Table 74: 10GBASE-KR TX

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Output Speed	–	–100 ppm	+10.3125	+100 ppm	Gbaud
Differential Resistance	R_{in}	80	100	120	Ω
Differential Output Voltage (pk-pk) based on 101010.. pattern	VOD	–	–	1200	mVp-p
Output Voltage (pk-pk) when TX is disabled	VOD	–	–	30	mVp-p
Common Mode Voltage	VCM	TBD	0.55	TBD	V
Differential Output Return Loss (min)	Equation[a]	–	–	–	dB
Common-mode Output Return Loss (min)	Equation[b]	–	–	–	dB
Output Rise Time (20%–80%)	Tr	24	–	47	pS
Output Fall Time (20%–80%)	Tf	24	–	47	pS
Output Jitter @ 1e-12 BER					
Random	sr	–	–	0.15	UI
Deterministic	sdt	–	–	0.15	UI
Duty Cycle Distortion	sdc	–	–	0.035	UI
Total	st	–	–	0.28	UI

a. Return Loss (f) ≥ 9 dB for 50 MHz ≤ f < 2500 MHz
Return Loss (f) ≥ [9−12log(f/2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz, where f is in Megahertz.
b. Return Loss (f) ≥ 6 dB for 50 MHz ≤ f < 2500 MHz
Return Loss (f) ≥ [6−12log(f/2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz, where f is in Megahertz.

Receiver

Table 75: 10GBASE-KR RX

Parameters	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Receiver Coupling	AC	0.05	–	0.1	µF
Differential Input Voltage (pk-pk)	VID	–	–	1200	mVp-p
Differential Input Return Loss (min)	Equation 1	–	–	–	dB
Receiving Speed	–	–100 ppm	+10.3125	+100 ppm	Gbaud
Differential Resistance	R_{in}	80	100	120	Ω

AC-JTAG

The serial interface AC-JTAG characteristics are shown in Table 76.

Table 76: Serial Interface AC-JTAG Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Fault Resistance Detect	R_{sc}	Short Circuit	0	–	5	Ω
	R_{oc}	Open Circuit	20	–	–	kΩ
Transmit Voltage Levels	V_{TX}	Differential p-p	0.5	1.0	1.3	V
Transmit Data Rate	–	EXTEST_TRAIN	1	–	30	Mbps
Output Resistance	R_{DRV}	DP or DM to VDD	–	50	–	Ω
Transmit Supply Current	I_{DD}	Operating mode	–	56	–	mA
Receiver Input Capacitance	C_{IN}	DP or DM to GND	–	0.5	0.6	pF
Common-Mode Voltage	V_{CM}	–	–	–	V_{DD}–0.2	V
Comparator Hysteresis[a]	V_{HYS}	Peak-to-peak	25	150	300	mV
Receive Data Rate	–	EXTEST_TRAIN	1	–	30	Mbps

a. Transmit voltage levels, as well as receiver hysteresis, are user programmable.

Table 77 and Table 78 show the AC-JTAG settings and the corresponding typical voltages.

Table 77: AC-JTAG Transmit Setting (Driver Bias Current)

Cfg Value	Transmit Amplitude [Vpp]	Cfg Value	Transmit Amplitude [Vpp]
0111	0.68	1111	1.04
0110	0.73	1110	1.06
0101	0.78	1101	1.07
0100	0.83	1100	1.08
0011	0.88	1011	1.08
0010	0.93	1010	1.09
0001	0.98	1001	1.09
0000	1.01	1000	1.10

Table 78: AC-JTAG Receive Configuration

Cfg Value	Rx Hysteresis (mVpp)	Cfg Value	Rx Hysteresis (mVpp)
111	130	011	0
110	100	010	300
101	70	001	230
100	40	000	170

Section 9: Thermal Characteristics

Table 79 shows the thermal characteristics of BCM56150 in 24x 1G + 4x 10G configuration at T_A=55°C with 35 x 35 x 25 mm^3 heatsink.

Table 79: 1006L - FCBGA + HS Thermal Characteristics with 35 x 35 x 25 mm^3 External Heat Sink at T_A = 55°C, P = 12.81W

Air Flow (LFPM)	*0*	*100*	*200*	*400*	*600*
Theta-$_{JA}$ (°C/W)	6.17	4.03	3.14	2.60	2.42
Theta-$_{JB}$ (°C/W)	3.62	–	–	–	–
Theta-$_{JC}$ (°C/W)	0.97	–	–	–	–
Maximum Junction Temperature T_J (°C)[a]	134.04	106.63	95.23	88.31	86.00
Heatsink: 35 mm x 35 mm x 25 mm					

a. Steady state junction temperature should not exceed 110 °C.

Table 80 shows the thermal characteristics of BCM56150 in 24x 1G + 2x 10G + 2x 13G configuration at T_A=55°C with 35 x 35 x 25 mm^3 heatsink.

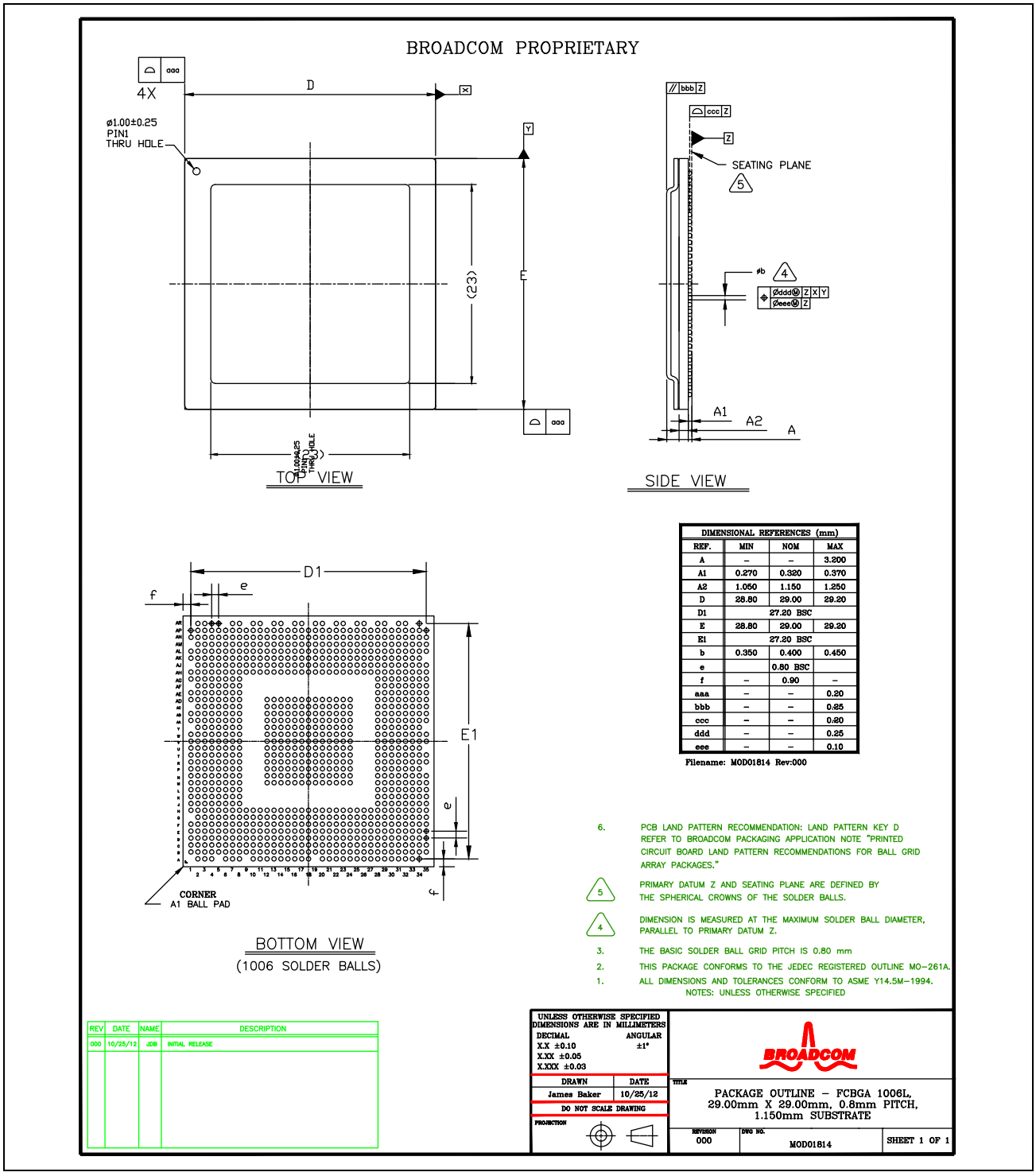
Table 80: 1006L - FCBGA + HS Thermal Characteristics with 35 x 35 x 25 mm^3 External Heat Sink at T_A = 55°C, P = 13.83W

Air Flow (LFPM)	*0*	*100*	*200*	*400*	*600*
Theta-$_{JA}$ (°C/W)	6.17	4.03	3.14	2.60	2.42
Theta-$_{JB}$ (°C/W)	3.62	–	–	–	–
Theta-$_{JC}$ (°C/W)	0.97	–	–	–	–
Maximum Junction Temperature T_J (°C)[a]	140.35	110.75	98.44	90.97	88.48
Heatsink: 35 mm x 35 mm x 25 mm					

a. Steady state junction temperature should not exceed 110 °C.

Section 10: Mechanical Information

Figure 67: 29 mm x 29 mm Package



Section 11: Ordering Information

Table 81: Ordering Information for RoHS6 Devices (Contact Broadcom for Availability)

Part Number	*Package*	*Description*	*Ambient Temperature*
BCM56150A0KFSBLG	1006-pin FCBGA +HS (29 mm x 29 mm) RoHS6 Compliant	24-Port Managed GbE Switch with 16 Copper PHYs and Four 10GbE Uplinks	0°C to 70°C
BCM56150A0IFSBLG	1006-pin FCBGA +HS (29 mm x 29 mm) RoHS6 Compliant	24-Port Managed GbE Switch with 16 Copper PHYs and Four 10GbE Uplinks	–40°C to 85°C

Table 82: Ordering Information for RoHS6 Devices with Exemption 15 (Eutectic Bumps Internally Between Die and Substrate)

Part Number	*Package*	*Description*	*Ambient Temperature*
BCM56150A0KFSBG	1006-pin FCBGA +HS (29 mm x 29 mm)	24-Port Managed GbE Switch with 16 Copper PHYs and Four 10GbE Uplinks	0°C to 70°C
BCM56150A0IFSBG	1006-pin FCBGA +HS (29 mm x 29 mm)	24-Port Managed GbE Switch with 16 Copper PHYs and Four 10GbE Uplinks	–40°C to 85°C

Appendix A: Acronyms and Abbreviations

For a more complete list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Term	*Description/Usage*
ACA	Accessory Charger Adapter
ACI	Adjacent Channel Interference
ACL	Access Control Logic
ACP	Accelerator Coherency Port
AH	Authentication
AHB	Advanced High Performance Bus
ALU	Arithmetic and Logic Unit 1. The unit of a computing system that contains the circuits that perform arithmetic operations. 2. A functional component of a computer system that performs arithmetic operations. See *vector unit* and *scalar unit*.
AOPC	Always-On Power Controller
APB	Advanced Peripheral Bus
AS	1. Autonomous System (ATM) 2. access stratum (3GPP)
ATB	Advanced Trace Bus
AUTN	authentication token (3GPP)
AXI	Advanced eXtensible Interface
BB	Baseband. (*Bluetooth*)
BBC	backup battery charger
BCCH	Broadcast Control Channel
BER	Bit Error Rate
BIF	Battery Interface (MIPI Alliance)
BMC	Best Master Clock
BPS	Bits-Per-Second
BSC	Broadcom Serial Control: A proprietary Broadcom bus or interface that is compatible with the Philips® I^2C bus or interface.
CC	1. Call Control. (*Bluetooth*) 2. Constant Current
CCBS	Completion of Calls to Busy Subscribers or Call Completion on Busy Subscriber
CCI	Camera Control Interface
CCP	Compact Camera Port
CCP2	Compact Camera Port 2 -
CCU	Clock Control Unit
CDP	1. compact display port 2. Charging Downstream Port

Term	*Description/Usage*
CFP	Compact Field Processor
CM	1. configuration management: The detailed recording and updating of information that describes an enterprise's computer systems and networks, including all hardware and software components. 2. congestion management 3. Connection Manager or Connection Management
CML	Common Mode Logic
CMSP	Content Management Service Provider
CoS	Class-of-Service
CPE	Customer Premise Equipment
CSI	Camera Serial Interface
CSI2	Camera Serial Interface 2 - 02/18/10
CSR	1. Control and Status Register 2. core switching regulator
CTI	cross trigger interface
CTM	Cross Trigger Matrix
CV	1. Credential Vault 2. Constant Voltage
DA	Destination Address
DAP	Debug Access Port
DBI	Display Bus Interface
DCP	Dedicated Charging Port
DCXO	Digitally Compensated Crystal Oscillator
DF	Don't Fragment
DigRF	Baseband/RF Digital interface specification
DLL	Data Link Layer
DLLP	Data Link Layer Packet
DMU	Device Management Unit
DoS	Denial of Service
DPI	Display Pixel Interface
DRM	1. Digital Rights Management 2. Digital Restrictions Management
DSI	1. Display Stream Interface: A high-speed serial interface for LCD modules. 2. Display Serial Interface
DT	Double Tag
DTE	Digital Timing Engine
DVFS	Dynamic Voltage and Frequency Scaling
DVS	Dynamic Voltage Scaling
EAPOL	Extensible Authentication Protocol over LAN
ECC	Error-Correction Code
ECRC	End-to-end CRC
ENS	Enhanced Network Selection (GPS)

Term	*Description/Usage*
ESP	Encapsulating Security Payload
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell (ARM® Microprocessors)
EVM	Error Vector Magnitude
FG	fuel gauge
GIC	General Interrupt Controller
GMM	GPRS Mobility Management
GPRS	General Packet Radio Service: A standard for wireless communications that run at speeds of up to 171 Kbps, compared with GSM systems, which run at 9.6 Kbps. GPRS, which supports a wide range of bandwidths, is an efficient use of limited bandwidth particularly suited for sending and receiving small bursts of data, such as for e-mail and Web browsing, as well as large volumes of data.
GSM	Global System for Mobile Communications: A second generation digital cellular technology developed by European countries in the 1980s to facilitate pan-European roaming. GSM uses time division multiple access technology and operates at both cellular and PCS frequencies (900 MHz, 1800 MHz, 1900 MHz). Other technologies used are CDMA, PDC & TDMA. In 1999, 66% of the world's cell phones were GSM (source: EMC World Cellular Database).
HOSTON	PMU state is on
HPLMN	Home Public Land Mobile Network
HSDPA	High-Speed Downlink Packet Access
HSUPA	High-Speed Upload Packet Access
HVS	Hardware Video Scaler
I^2S	1. Inter-IC Sound 2. Integrated Interchip Sound 3. Internet Information Server (*Microsoft*) Electrical serial bus interface standard for connecting digital audio devices. Up to 16 audio channels at up to 192 kHz.
IDT	Intelligent Double Tag
IF	1. interface 2. Intermediate Frequency: A frequency below Radio Frequency (RF). In a GPS receiver, the RF chip converts the analog RF signal to IF and then converts it to a digital signal that is processed by the baseband device.
IHL	Internet Header Length
IMSI	International Mobile Subscriber Identity
IOSR	Input/Output Service Request
ISI	Intersymbol Interference
ITM	Instruction Trace Module
ITU	International Telecommunications Union
LA	Location Area
LAI	Location Area Identification
LDO	1. Low-Dropout 2. low dropout regulator
Li-ion	Lithium ion battery

Term	*Description/Usage*
LNA	low noise amplifier: Analog radio amplifier, used as the first stage in a GPS front-end. The GL-LN22 RF chip contains an integrated LNA on-chip.
LPM	1. Longest Prefix Match: IP packet forwarding mechanism. 2. Longest Prefix Match: An algorithm used by routers in Internet Protocol (IP) networking to select an entry from a routing table. 3. low power mode
MBC	main battery charger
MBRDY	PMU state is off but it is ready to turn on
MBWV	Main Battery Working Voltage
MEMC	memory controller
MF	More Fragments
MIDI	Musical Instrument Digital Interface
MIPI	Mobile Industry Processor Interface
MLC	Multi-Level Cell
MM	1. multimedia 2. Mixed Mode 3. ESD Machine Model
MMA	Mobility Management Adaptation
MME	Mobility Management Entity
MMR	Mobility Management Router
MS	1. mobile station: Refers to the handset or mobile wireless device in a C-plane architecture. 2. mobile subscriber
MSTP	Multiple Spanning Tree Protocol
MTT	Mobile Trace Terminal
NCO	Numerically Controlled Oscillator
NM	normal mode
NNI	Service-Provider Network Interface
NTC	Negative Temperature Coefficient
OAM	Operations, Administration, and Maintenance
OCP	Open Core Protocol
ONFI	Open NAND Flash Interface
OTG	On-the-Go
P-TMSI	Packet Temporary Mobile Subscriber Identity (GSM 03.60 version 7.4.1)
PA	power amplifier
PCGUI	Phone Control Graphical User Interface
PCIe™	PCI Express®
PCP	Priority Code Point
PD	1. Protocol Discriminator (GPRS LLC-layer address field format) - 2. Phase Detector
PDM	pulse density modulation
PDP	Packet Data Protocol

Term	*Description/Usage*
PDU	protocol data unit 1. OSI term for packet. 2. Information that is delivered as a unit between peer entities of a LAN or a MAN and contains control information, address information, and may contain user data. 3. A block of data that is exchanged between two devices using a protocol.
PHY	Physical Layer
PIM	1. Protocol-Independent Multicast: Multicast routing architecture that allows the addition of IP multicast routing protocols. Packets are forwarded on all outgoing interfaces until pruning and truncation occur. In dense mode, receivers are densely populated, and it is assumed that the downstream networks want to receive and will use the datagrams that are forwarded to them. The cost of using dense mode is its default flooding behavior. Sometimes referred to as Dense Mode PIM or PIM DM. Contrast with PIM Sparse Mode. 2. personal information manager 3. personal information management
PLMN	Public Land Mobile Network
PMM	1. Packet Mobility Management (in GPRS) 2. Performance Measurement Matrix 3. Pressurized Multipurpose Module
PMU	Power Management Unit
PPS	Packet-Per-Second
PSMS	Power System Monitoring and Simulation
PSRR	Power Supply Rejection Ratio
PTI	Parallel Trace-Data Interface
PTM	Program Trace Macrocell
PWM	Pulse-Width Modulator
PWRUP	PMU state is off and it is not ready to turn on
QoS	Quality of Service
RAI	Routing Area Identification
RNTI	Radio Network Temporary Identifier (3GPP)
RPLMN	Registered Public Land Mobile Network
RR	Radio Resource
RTOS	Real-time Operating Systems
RV	Rate Violation
S/PDIF	Sony/Philips Digital Interconnect Format
SAIC	Single Antenna Interference Cancellation
SCU	Snoop Control Unit
SDIO	Secure Digital Input/Output
SDP	1. Service Discovery Protocol 2. Session Description Protocol 3. Sockets Direct Protocol 4. Standard Downstream Port
SDSR	SD switching regulator
SLC	Single-Level Cell

Term	*Description/Usage*
SP	Strict Priority
SS	Supplementary Services
STM	System Trace Module
STP	System Trace Protocol
SWD	Serial Wire Debug
TBF	Temporary Block Flow
TC	Traffic Class
TL	Transaction Layer
TLB	Translation Lookaside Buffer
TLLI	Temporary Logical Link Identity (GPRS protocols, LLC layer)
TLP	Transaction Layer Packet
TOS	Type Of Service
TPID	Tag Protocol ID
TPIU	Trace Port Interface Unit
TTL	Time To Live
UDFs	User-Defined Fields
UMI	Unified Memory Interface
UMTS	Universal Mobile Telecommunications System: The third generation mobile standards that will build on the success of GSM/GPRS and on the GSM operators' existing investment in infrastructure. Data rates offered will be up to 2 million bits per second.
UNI	User Network Interface
USBC	USB charger
USIM	1. User Services Identity Module (UMTS) 2. Universal Mobile Telecommunications System 3. UMTS subscriber identity mode
USIMAP	USIM application process
UTRAN	UMTS Terrestrial Radio Access Network: A conceptual term identifying that part of the network which consists of Radio Network Controllers and Node Base stations.
VID	VLAN ID
VLAN	Virtual LAN
VMBAT	Main Battery Voltage
WAC	wall adapter charger
WDT	watchdog timer
WRR	Weighted-Round-Robin
XIP	Execute in Place

Broadcom Corporation
5300 California Avenue
Irvine, CA 92617

Phone: 949-926-5000
Fax: 949-926-5203
E-mail: info@broadcom.com
Web: www.broadcom.com